MCP201

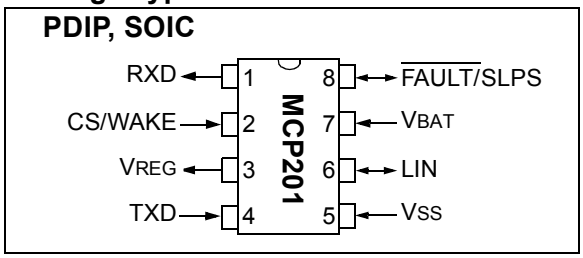
LIN Transceiver with Voltage Regulator

Features

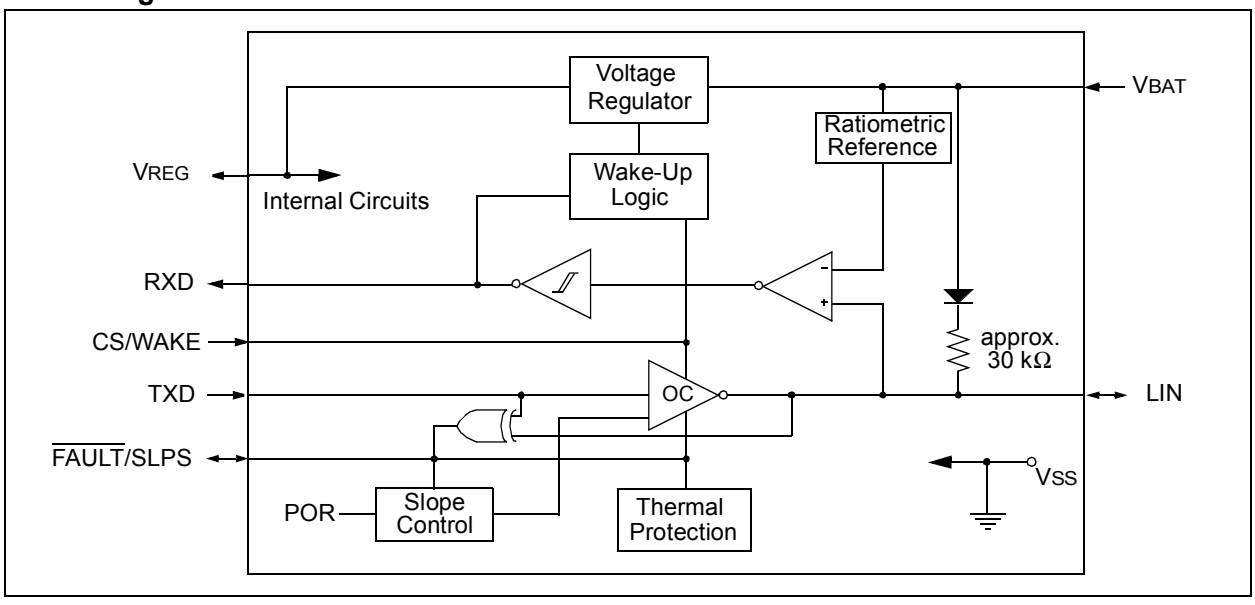
- Support Baud Rates up to 20 kbaud
- 40V load dump protected
- Wide supply voltage, 6.0 - 18.0V, continuous
  - Maximum input voltage of 30V
- Extended Temperature Range: -40 to +125°C
- Interface to standard USARTs
- Compatible with LIN Spec 1.3
- Local Interconnect Network (LIN) Line pin:
  - Internal pull-up resistor and diode
  - Protected against ground shorts (LIN pin to ground)
  - Protected against LIN pin loss of ground
  - High current drive, 40 mA ≤ I_{OL} ≤ 200 mA
- Automatic thermal shutdown
- On-board Voltage Regulator:
  - Output voltage of 5V with ±5% tolerances over temperature range
  - Maximum output current of 50 mA
  - Able to drive an external series-pass transistor for increased current supply capability
  - Internal thermal overload protection
  - Internal short-circuit current limit
  - External components limited to filter cap only

Package Types

PDIP, SOIC



Block Diagram



NOTES:

1.0 DEVICE OVERVIEW

The MCP201 provides a physical interface between a microcontroller and a LIN half-duplex bus. It is intended for automotive and industrial applications with serial bus speeds up to 20 kbaud.

The MCP201 provides a half-duplex, bidirectional communications interface between a microcontroller and the serial network bus. This device will translate the CMOS/TTL logics levels to LIN level logic, and vice versa.

The LIN specification 1.3 requires that the transceiver of all nodes in the system be connected via the LIN pin, referenced to ground and with a maximum external termination resistance of 510Ω from LIN bus to battery (510Ω is the maximum load of the LIN bus, which corresponds to one Master and 16 Slave nodes).

The MCP201 provides a +5V 50 mA regulated power supply. This function is short-circuit-protected and it can generate a thermal shutdown. The regulator has been specifically designed to operate in the automotive environment and will survive reverse battery connections, +40V load dump transients, and double-battery jumps (see Section 1.6, “Internal Voltage Regulator”).

1.1 Optional External Protection

1.1.1 TRANSIENT VOLTAGE PROTECTION (LOAD DUMP)

An external 30V zener diode, between VBAT and ground, with a 50Ω resistor in series with the battery supply and the VBAT pin serve to protect the device from power transients (see Figure 1-2).This protection is optional, but should be considered as good engineering practice.

1.1.2 REVERSE BATTERY PROTECTION

An external reverse battery blocking diode can be used to provide polarity protection (see Figure 1-2). This protection is optional, but should be considered as good engineering practice.

1.2 Internal Protection

1.2.1 ESD PROTECTION

This device meets IEC 1000-4-2:1995 specifications.

1.2.2 GROUND LOSS PROTECTION

The LIN bus specification states that an inactive node must assume the recessive state. Therefore, loss of ground effectively forces the LIN line to a hi-impedance level.

1.2.3 THERMAL PROTECTION

The thermal protection circuit monitors the die temperature and is able to shut down the LIN transmitter and voltage regulator. Refer to Table 1-1 for details.

There are two sources for a thermal overload. One is the voltage regulator, which can have an output overload. The other is the LIN transmitter with a short-circuit to VBAT. Checking the TXD and RXD states make it possible to determine the thermal excursion source and to shut it down.

TABLE 1-1: SOURCES OF THERMAL OVERLOAD

TXD	RXD	LIN Transmitter(1)	Voltage Regulator(2)	Comments
x	x	ok	ok	Normal function
L	L	output overload	output overload	LIN transmitter and regulator shutdown
L	H	short circuit	ok	LIN transmitter shutdown
H	H/L	ok	output overload	Regulator shutdown

Legend: x = Don’t care, L = Low, H = High

Note 1: LIN transceiver overload current on the LIN pin is > 200 mA.

2: Voltage regulator overload current on VREG is > 50 mA.

1.3 Modes of Operation

For an overview of all operational modes, please refer to Table 1-2.

1.3.1 POWER-DOWN MODE

In the Power-Down mode, the transmitter and the voltage regulator are both off. Only the receiver section and the CS/WAKE pin wake-up circuits are in operation. This is the lowest power mode.

If any bus activity (e.g., a BREAK character) should occur during Power-Down mode, the device will immediately enable the voltage regulator. Once the output has stabilized, enter the Ready mode.

The part will enter the operation mode if the CS/WAKE pin should become active-high (‘1’).

1.3.2 READY MODE AND READY1 MODE

There are two states for the Ready mode.The only difference between these states is the transition during start-up of the regulator, depending on the signal CS/WAKE. The state Ready1 mode ensures that the transition from the Ready-to-Operation mode (once an active edge of CS/WAKE) occurs.

Upon entering the Ready mode, the voltage regulator is powered up. If a microcontroller is being driven by the voltage regulator output, it will go through a power-on reset and initialization sequence. All other circuits, other than the transmitter, are fully operational. The LIN pin is held in the recessive state.

The device will stay in the Ready mode until the CS/WAKE pin goes high (‘1’). After CS/WAKE is active, the transmitter is enabled and the part enters the Operation mode.

The part may only enter the Power-Down mode after going through an Operation mode step.

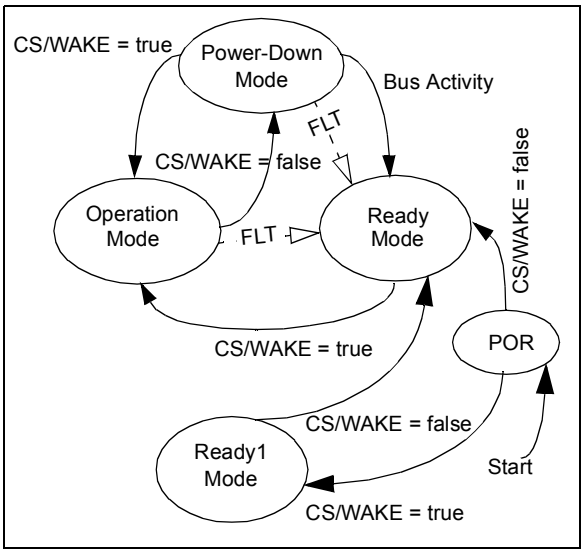
On power-on of the V_{BAT} supply pin, the component is in either in Ready or Ready1 mode, waiting for a CS/WAKE rising edge.

1.3.3 OPERATION MODE

In this mode, all internal modules are operational.

The MCP201 will go into the Power-down mode on the falling edge of CS/WAKE.

FIGURE 1-1: OPERATIONAL MODES STATE DIAGRAMS



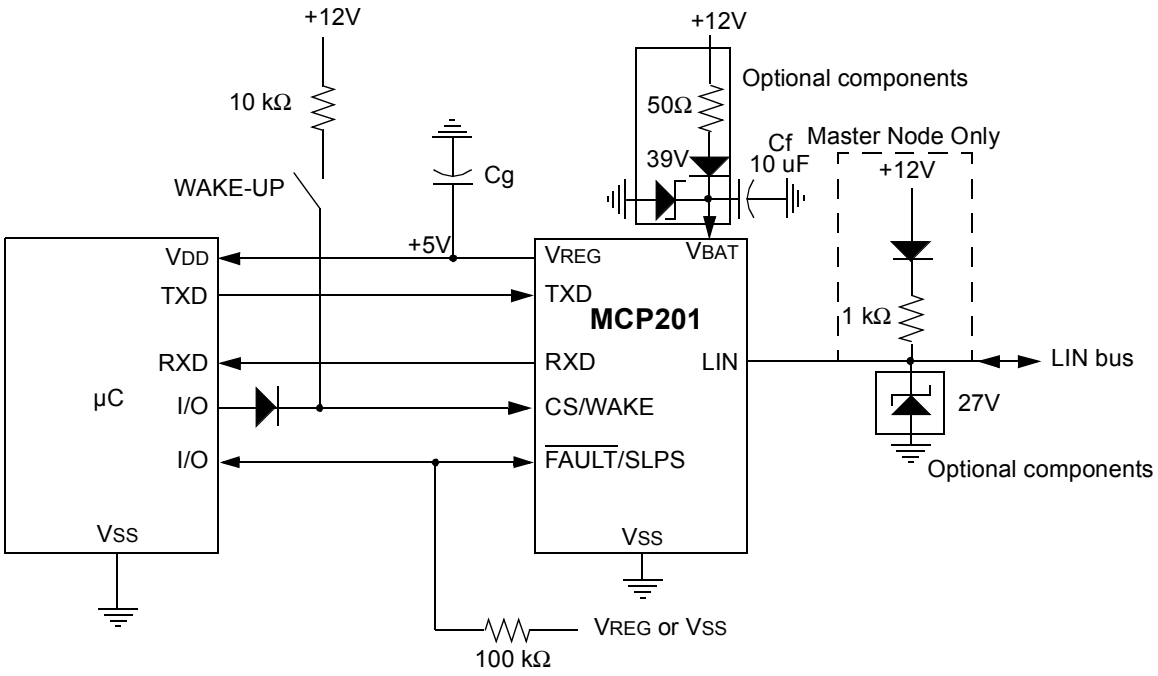
Note:	While the MCP201 is in shutdown, TXD should not be activaly driven high.

TABLE 1-2: OVERVIEW OF OPERATIONAL MODES

State	Transmitter	Voltage Regulator	Operation	Comments
POR	OFF	OFF	Read CS/WAKE, if LOW then READY, if HIGH READY1 mode	Sample FAULT/SLPS and select slope
READY	OFF	ON	If CS/WAKE rising edge, then Operation mode	Bus Off state
READY1	OFF	ON	If CS/WAKE falling edge, then READY mode	Bus Off state
OPERATION	ON	ON	If CS/WAKE falling edge, then Power down	Normal Operation mode
POWER-DOWN	OFF	OFF	On LIN bus falling, go to READY mode. On CS/WAKE rising edge, go to Operational mode	Low Power mode

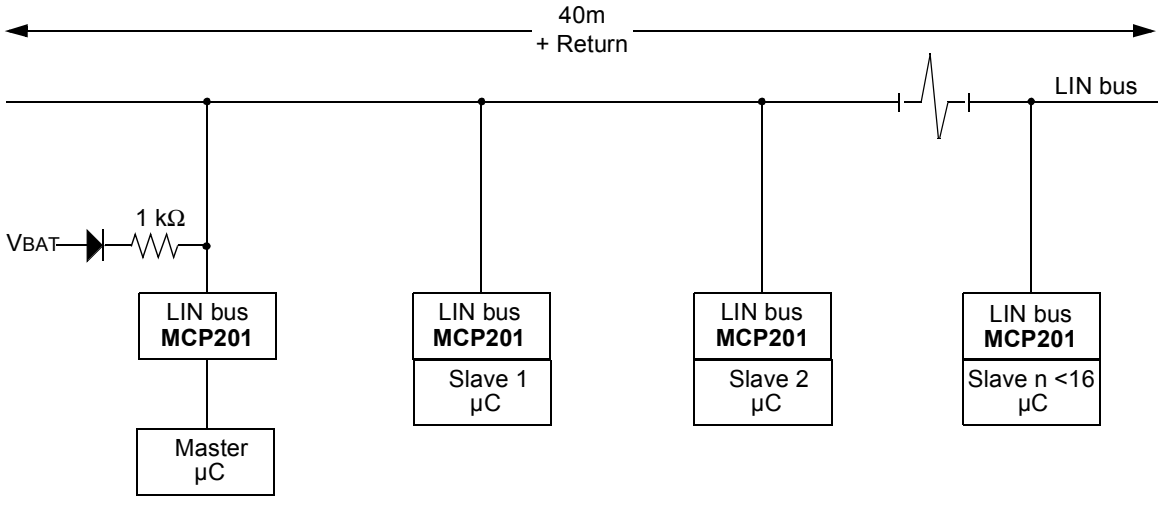
1.4 Typical Applications

FIGURE 1-2: TYPICAL MCP201 APPLICATION



Note 1: Cg is the load capacitor for the internal voltage regulator.
Note 2: Cf if the filter capacitor for the external voltage supply.

FIGURE 1-3: TYPICAL LIN NETWORK CONFIGURATION



1.5 Pin Descriptions

TABLE 1-3: MCP201 PINOUT OVERVIEW

Bondpad Name	Devices		Function
	8-Pin PDIP	8-Pin SOIC	Normal Operation
RXD	1	1	Receive Data Output
CS/WAKE	2	2	Chip Select (TTL-HV)
V_{REG}	3	3	Power Output
TXD	4	4	Transmit Data Input (TTL)
V_{SS}	5	5	Ground
LIN	6	6	LIN bus (bidirectional-HV)
V_{BAT}	7	7	Battery
$\overline{FAULT}$/SLPS	8	8	Fault Detect Output, Slope Select Input
Total	8	8	

Legend: TTL = TTL input buffer,
HV = High Voltage (V_{BAT})

1.5.1 POWER OUTPUT (V_{REG})

Positive Supply Voltage Regulator Output pin. The voltage output from the regulator also supplies power to internal logic.

1.5.2 GROUND (V_{SS})

Ground pin.

1.5.3 BATTERY (V_{BAT})

Battery Positive Supply Voltage pin. This pin is also the input for the internal voltage regulator.

1.5.4 TRANSMIT DATA INPUT (TXD)

Transmit Data Input pin. This pin has an internal pull-up to V_{REG}. The LIN pin is low (dominant) when TXD is low, and high (recessive) when TXD is high.

1.5.5 RECEIVE DATA OUTPUT (RXD)

Receive Data Output pin. This pin is a standard CMOS output, and follows the state of the LIN pin.

1.5.6 LIN

Bidirectional LIN bus Interface pin.

1.5.6.1 LIN Transmitter

The LIN Transmitter is the driver unit for the LIN pin and is controlled by the signal TXD. It has an open collector output with a current limitation. To reduce EMI, the edges during the signal changes are slope controlled.

In case the thermal protection detects an over-temperature condition while the signal TXD is LOW, the transmitter is shutdown. The recovery from the thermal shutdown is equal to adequate cooling time.

1.5.6.2 LIN Receiver

The LIN Receiver monitors the state of the LIN pin and generates the output signal RXD.

1.5.6.3 CS/WAKE

Chip Select Input pin. When CS = '1', the transmitter and the voltage regulator are both enabled.

If CS/WAKE = '0', the device is in Ready mode on power-up or in Low Power mode. In Low Power mode, the voltage regulator is shutdown and the transmitter driver is enabled. The internal pull-down resistor will keep the CS/WAKE pin low. This is done to ensure that no disruptive data will be presented on the bus while the microcontroller is executing a Power-on Reset and I/O initialization sequence.

The internal pull-down resistor will keep the input low. An external switch (or other source) can then wake up both the transceiver and the microcontroller. An external-blocking diode and current-imiting resistor are necessary to protect the microcontroller I/O pin (see Figure 1-2).

Note:	On POR, the MCP201 enters Ready or Ready1 mode (see Figure 1-1). In order to enter Operational mode, the MCP201 has to see one rising edge on CS.

1.5.7 $\overline{\text{FAULT}}$/SLPS

FAULT Detect Output, Slope Select Input.

This pin is usually in Output mode. Its state is defined as shown in Table 1-5.

The state of this pin is internally sampled during power-on of V_{BAT}. Once V_{BAT} has reached a stable level (approx. 6 VDC) and V_{REG} is stable at 4.75-5.25 VDC, the state of this pin selects which slew rate profile to apply to the LIN output. It is only during this time that the pin is used as an input (the output driver is off during this time). The slope will stay selected until the next V_{BAT} power-off/power-on sequence, regardless of any power-down, wake-up or SLEEP events. Only a V_{BAT} rising state will cause a sampling of the $\overline{\text{FAULT}}$/SLPS pin. The Slope selection will be made irrespective of the state of any other pin.

The $\overline{\text{FAULT}}$/SLPS pin is connected to either V_{REG} or V_{SS} through a (approx. 100 kΩ) resistor to make the slope selection. This large resistance allows the FAULT indication function to overdrive the resistor in normal operation mode.

If the $\overline{\text{FAULT}}$/SLPS is high ('1'), the normal slope shaping is selected (dv/dt = 2 V/µs). If $\overline{\text{FAULT}}$/SLPS is low ('0') during this time, the alternate slope shaping is selected (dv/dt = 4 V/µs)

TABLE 1-4: $\overline{\text{FAULT}}$/SLPS SLOPE SELECTION DURING POR

$\overline{\text{FAULT}}$/SLPS	Slope Shaping
H	Normal
L	Alternate(1)

Note 1: This mode does not conform to LIN bus specification Ver. 1.3.

Note: This pin is '0' whenever the internal circuits have detected a short or thermal excursion and have disabled the LIN output driver.

Note: Every time TX is toggled, a Fault condition will occur for the length of time, depending on the bus load. The Fault time is equal to the propagation delay.

TABLE 1-5: $\overline{\text{FAULT}}$/SLPS TRUTH TABLE

TXD In	RXD Out	LIN bus I/O	Thermal Override	$\overline{\text{FAULT}}$/SLPS Out	Comments
L	H	V_{BAT}	OFF	L	Bus shorted to battery
H	H	V_{BAT}	OFF	H	Bus recessive
L	L	GND	OFF	H	Bus dominant
H	L	GND	OFF	L	Bus shorted to ground
x	x	V_{BAT}	ON	L	Thermal excursion

Legend: x = don't care

1.6 Internal Voltage Regulator

The MCP201 has a low drop-out voltage, positive regulator capable of supplying 5.00 VDC ±5%, at up to 50 mA of load current over the entire operating temperature range. With a load current of 50 mA, the minimum input-to output voltage differential required for the output to remain in regulation is typically +0.5V (+1V maximum over the full operating temperature range). Quiescent current is less than 1.0 mA, with a full 50 mA load current, when the input-to-output voltage differential is greater than +2V.

The regulator requires an external output bypass capacitor for stability.

Designed for automotive applications, the regulator will protect itself, any load from reverse battery connections, double-battery jumps and up to +40V load dump transients. The voltage regulator has both short-circuit and thermal shutdown protection built-in.

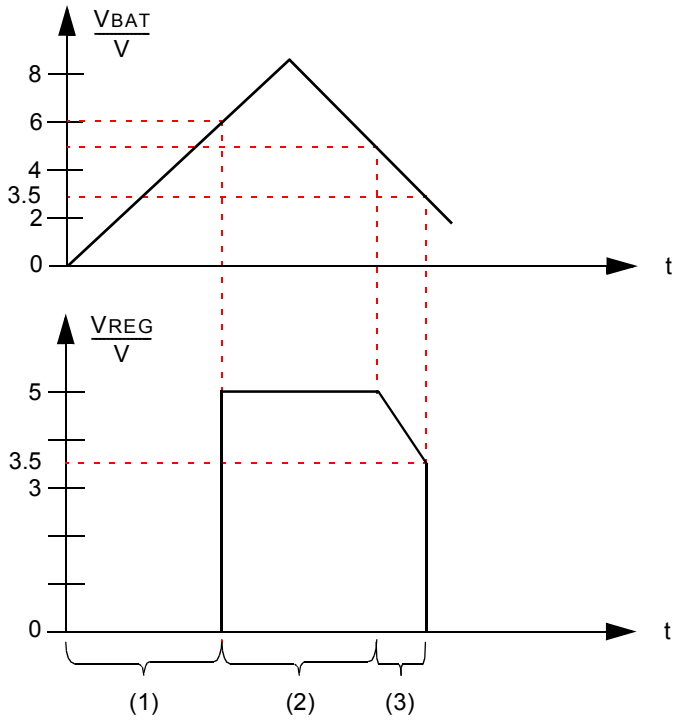
Regarding the correlation between VBAT, VREG and IDD, please refer to Figure 1-4 through Figure 1-7. When the input voltage (VBAT) drops below the differential needed to provide stable regulation, the output VREG will track the input down to approximately 4V, at which point the regulator will turn off. This will allow microcontrollers with internal POR circuits to generate a clean arming of the Power-on Reset trip point. The regulator output will stay off until VBAT is above, approximately, 6V.

In the start phase, VBAT must be at least 6.0V (Figure 1-4) to initiate operation during power-up. In Power-down mode, the VBAT monitor will be turned off.

The regulator has a thermal shutdown. If the thermal protection circuit detects an over-temperature condition caused by an over-current condition (Figure 1-7) of the regulator, it will shutdown.

The regulator has an overload current limiting. During a short-circuit, VREG is monitored. If VREG is lower than 3.5V, the regulator will turn off. After a thermal recovery time, the VREG will be checked again. If there is no short-circuit (VREG > 3.5V), the regulator will be switched back on.

FIGURE 1-4: VOLTAGE REGULATOR OUTPUT ON POWER-ON RESET

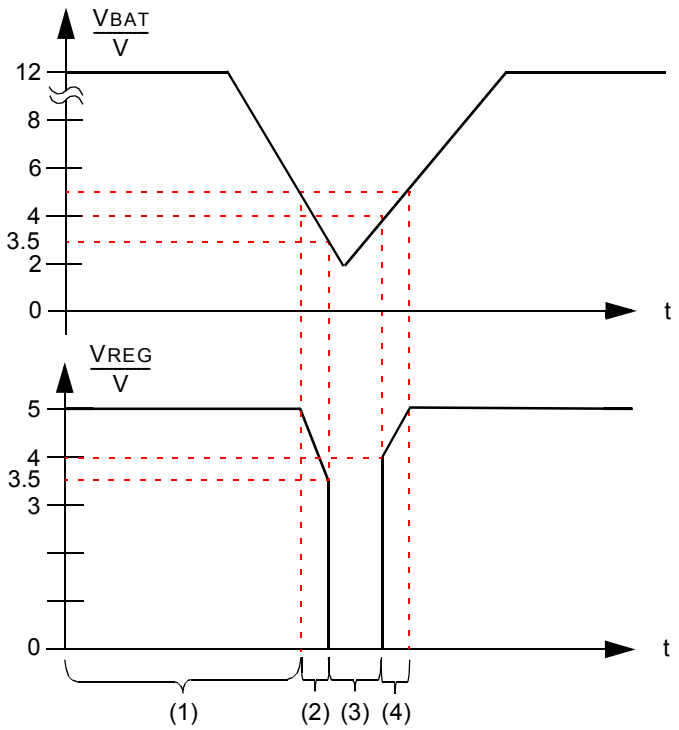


Note 1: Start-up, VBAT < 6.0V, regulator off.

2: VBAT > 6.0V, regulator on.

3: VBAT ≤ 5.5V, regulator tracks VBAT, regulator will turn off when VREG < 3.5V.

FIGURE 1-5: VOLTAGE REGULATOR OUTPUT ON POWER DIP



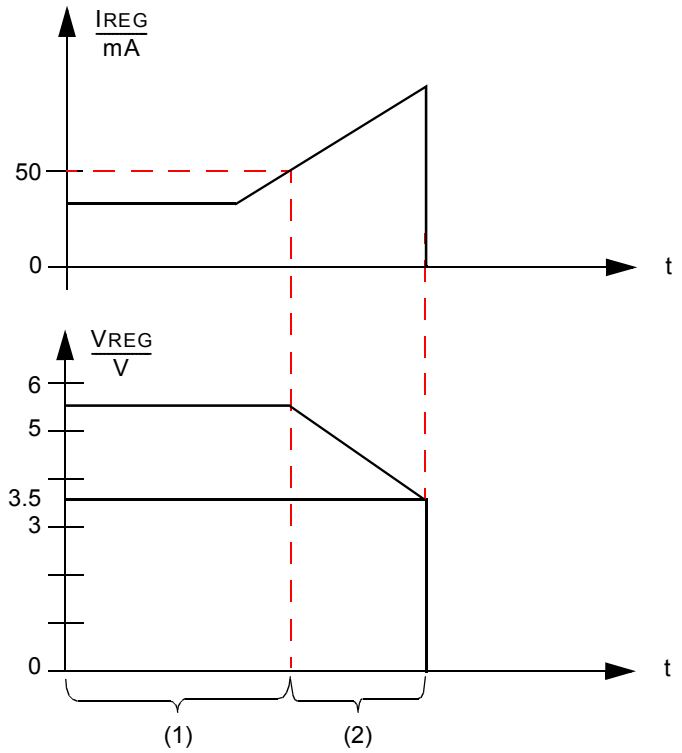
Note 1: Voltage regulator on.

2: $V_{REG} \leq 5.5V$, regulator tracks V_{BAT} until Vreg < 3.5V.

3: $V_{REG} < 3.5V$, regulator is off.

4: $V_{REG} > 4.0V$, voltage regulator tracks V_{DD}, when $V_{REG} > 4.0V$.

FIGURE 1-6: VOLTAGE REGULATOR OUTPUT ON OVER CURRENT SITUATION



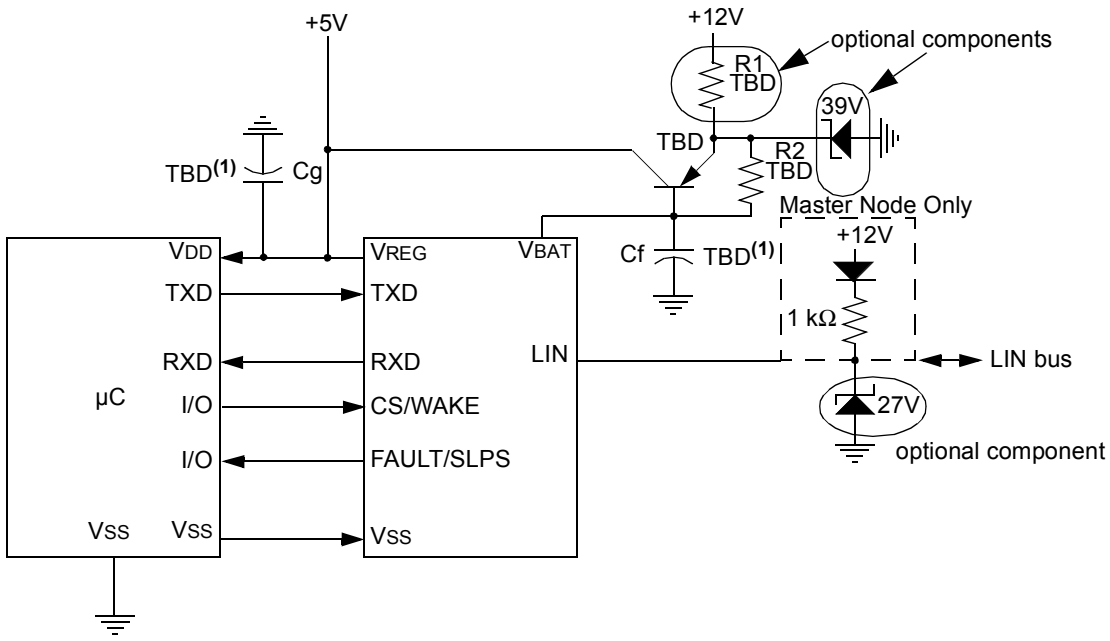
Note 1: IREG less than 50 mA, regulator on.

2: After IREG exceeds IREGmax, voltage regulator output will be reduced until VREGoff is reached.

1.6.1 INCREASED CURRENT CAPABILITY

In order to support applications requiring more than 50 mA, the regulator will support the addition of an external series pass transistor in a current-sharing configuration, as shown in Figure 1-7.

FIGURE 1-7: INCREASING CURRENT CAPABILITY WITH AN EXTERNAL TRANSISTOR



Note 1: Determined by application.

NOTES:

2.0 ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings†

V_{IN} DC Voltage on Logic pins except CS/WAKE ..... -0.3 to V_{REG}+0.3V

V_{IN} DC Voltage on CS/WAKE ..... -0.3 to V_{BAT}+0.3V

V_{BAT} Battery Voltage, non-operating (LIN bus recessive, no regulator load, t<60s)..... -0.3 to +40V

V_{BAT} Battery Voltage, transient (**Note 1**)..... -0.3 to +40V

V_{BAT} Battery Voltage, continuous ..... -0.3 to +30V

V_{LBUS} Bus Voltage, continuous..... -18 to +30V

V_{LBUS} Bus Voltage, transient (**Note 1**)..... -27 to +40V

I_{LBUS} Bus Short Circuit Current Limit ..... 200 mA

ESD protection on all pins (Human Body Model)..... >2 kV

ESD protection on all pins (Machine Model)..... >200V

Maximum Junction Temperature ..... 150°C

Storage Temperature ..... -55 to +150°C

Note 1: ISO 7637/1 load dump compliant (t < 500 ms).

† NOTICE: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2.2 DC Specifications

DC Specifications		Electrical Characteristics: Unless otherwise indicated, all limits are specified for: V_{BAT} = 6.0V to 18.0V; T_{AMB} = -40°C to +125°C; $C_{LOADREG}$ = 1 µF				
Symbol	**Parameter**	**Min**	**Typical**	**Max**	**Units**	**Conditions**
	Power					
I_{BATQ}	V_{BAT} Quiescent Operating Current	—	0.45	1.0	mA	I_{VREG}=0 mA, LIN bus pin recessive, (**Note 3)**
I_{BAT}	V_{BAT} Power-Down Current	—	23	50	µA	
I_{DDQ}	VREG Quiescent Operating Current	—	500	—	mA	(**Note 2**)
	Microcontroller Interface					
V_{IH}	High-Level Input Voltage (TXD, $\overline{FAULT}$/SLPS)	2.0	—	V_{REG} + 0.3	V	
V_{IL}	Low-Level Input Voltage (TXD, $\overline{FAULT}$/SLPS)	-0.3	—	0.15 x V_{REG}	V	
I_{IHTXD}	High-Level Output Current (TXD)	-90	—	+30	µA	Input voltage = 4V
I_{ILTXD}	Low-Level Output Current (TXD)	-150	—	-10	µA	Input voltage = 1V (though >50 kΩ internal pull-up)
$V_{IHCS/WAKE}$	High-Level Input Voltage (CS/WAKE)	3.0	—	V_{BAT}	V	Through an external current-limiting resistor (10 kΩ)
$V_{ILCS/WAKE}$	Low-Level Input Voltage (CS/WAKE)	-0.3	—	1.0	V	
$I_{IHCS/WAKE}$	High-Level Input Current (CS/WAKE)	-10	—	+80	µA	Input voltage = 4 V (though >100 kΩ internal pull-up)
$I_{ILCS/WAKE}$	Low-Level Input Current (CS/WAKE)	5	—	30	µA	Input voltage = 1V
V_{OHRXD}	High-Level Output Voltage (RXD)	0.8 V_{REG}	—	—		I_{OH} = -4 mA
V_{OLRXD}	Low-Level Output Voltage (RXD)	—	—	0.2 V_{REG}		I_{OL} = 4 mA
	Bus Interface					
V_{IHLBUS}	High-Level Input Voltage (L_{BUS})	0.6 V_{BAT}	—	18	V	Recessive state
V_{ILLBUS}	Low-Level Input Voltage (L_{BUS})	-8	—	0.4 V_{BAT}	V	Dominant state
V_{HYS}	Input Hysteresis	0.05 V_{BAT}	—	0.1 V_{BAT}	V	V_{IH} - V_{IL}
I_{OL}	Low-Level Output Current (L_{BUS})	40	—	200	mA	Output voltage = 0.1 V_{BAT}, V_{BAT} = 12 V
I_O	High-Level Output Current (L_{BUS})	-20	—	20	µA	V_{BUS} >= V_{BAT}, V_{LBUS} < 40V
I_P	Pull-up Current on Input (L_{BUS})	-180	—	-60	µA	Approx 30 kΩ internal pull-up @ V_{IH} = 0.7 V_{BAT}

Note 1: Internal current limited. 2.0 ms maximum recovery time (R_{LBUS} = 0Ω, TX = 0.4 V_{REG}, V_{LBUS} = V_{BAT}).

2: For design guidance only, not tested.

3: This current is at the V_{BAT} pin.

2.2 DC Specifications (Continued)

DC Specifications		Electrical Characteristics: Unless otherwise indicated, all limits are specified for: V_{BAT} = 6.0V to 18.0V T_{AMB} = -40°C to +125°C $C_{LOADREG}$ = 1 µF				
Symbol	**Parameter**	**Min**	**Typical**	**Max**	**Units**	**Conditions**
I_{SC}	Short-Circuit Current-Limit	50	—	200	mA	(**Note 1**)
V_{OH}	High-Level Output Voltage (L_{BUS})	0.8 V_{BAT}	—	—	V	
V_{OL}	Low-Level Output Voltage (L_{BUS})	—	—	0.2 V_{BAT}	V	

Note 1: Internal current limited. 2.0 ms maximum recovery time (R_{LBUS} = 0Ω, TX = 0.4 V_{REG}, V_{LBUS} = V_{BAT}).

2: For design guidance only, not tested.

3: This current is at the V_{BAT} pin.

2.2 DC Specifications (Continued)

DC Specifications		Electrical Characteristics: Unless otherwise indicated, all limits are specified for: V_{BAT} = 6.0V to 18.0V T_{AMB} = -40°C to +125°C $C_{LOADREG}$ = 1 µF				
Symbol	**Parameter**	**Min**	**Typical**	**Max**	**Units**	**Conditions**
	Voltage Regulator					
V_{REG}	Output Voltage	4.75	—	5.25	V	0 mA > I_{OUT} > 50 mA, 7.0V < V_{BAT} < 18V
V_{REG1}	Output Voltage	4.4	—	5.25	V	0 mA > I_{OUT} > 50 mA, 6.0V < V_{BAT} < 7.0V
ΔV_{REG1}	Line Regulation	—	10	50	mV	I_{OUT} = 1 mA, 7.0V < V_{BAT} < 18V
ΔV_{REG2}	Load Regulation	—	10	50	mV	5 mA < I_{OUT} < 50 mA, V_{BAT} = Constant
V_N	Output Noise Voltage	—	—	400	μV_{RMS}	1 V_{RMS} @ 10 Hz - 100 kHz
V_{SD}	Shutdown Voltage (monitoring V_{REG})	3.5	—	4.0	V	See **Figure 1-4**
V_{ON}	Input Voltage to Turn On Output (monitoring V_{BAT})	5.5	—	6.0	V	

Note 1: Internal current limited. 2.0 ms maximum recovery time (R_{LBUS} = 0Ω, TX = 0.4 V_{REG}, V_{LBUS} = V_{BAT}).

2: For design guidance only, not tested.

3: This current is at the V_{BAT} pin.

2.3 AC Specifications

AC Specifications		Electrical Characteristics: Unless otherwise indicated, all limits are specified for: V_{BAT} = 6.0V to 18.0V, T_{AMB} = -40°C to +125°C				
Symbol	**Parameter**	**Min**	**Typical**	**Max**	**Units**	**Conditions**
	Bus Interface					
|dV/dt|	Slope Rising and Falling Edges	1.0	2.0	3.0	V/µs	(40% to 60%), No Load
|dV/dt|	Slope Rising and Falling edges ALTERNATE	2.0	4.0	6.0	V/µs	(**Note 1**), No Load
$t_{TRANSPD}$	Propagation Delay of Transmitter	—	—	6.0	µs	t_{RECPD} = max
t_{RECPD}	Propagation Delay of Receiver	—	—	6.0	µs	(t_{RECPDR} or t_{RECPDF})
t_{RECSYM}	Symmetry of Propagation Delay of Receiver Rising Edge with Respect to Falling Edge	-2.0	—	2.0	µs	t_{RECSYM} = max
$t_{TRANSSYM}$	Symmetry of Propagation Delay of Transmitter Rising Edge with Respect to Falling Edge	-2.0	—	2.0	µs	$t_{TRANSSYM}$ = max ($t_{TRANSPDF}$ - $t_{RANSPDR}$)
	Voltage Regulator					
t_{BACTVE}	Bus Activity to Voltage Regulator Enabled	10	—	40	µs	Bus debounce time
t_{VEVR}	Voltage Regulator Enabled to Ready	—	50	200	µs	(**Note 2**)
$t_{VREGPOR}$	Voltage Regulator Enabled to Ready after POR	—	—	2.5	ms	(**Note 2**) C_{LOAD} = 25 nF
t_{CSOR}	Chip-Select to Operation Ready	0	50	200	µs	(**Note 2**)
t_{CSPD}	Chip-Select to Power-down	0	—	40	µs	(**Note 2**) No C_{LOAD}
$t_{SHUTDOWN}$	Short-Circuit to Shutdown	—	450	—	µs	Characterized but not tested
tSCREC	Short-Circuit Recovery Time	—	3.0	—	ms	Characterized but not tested

Note 1: The mode does not conform to LIN Bus specification version 1.3.

2: Time depends on external capacitance and load.

TABLE 2-1: MCP201 THERMAL SPECIFICATIONS

Sym	Parameter	Min	Typical	Max	Units	Test Conditions
$\theta_{RECOVERY}$	Recovery Temperature (junction temperature)	—	+135	—	°C	Characterized but not tested
$\theta_{SHUTDOWN}$	Shutdown Temperature (junction temperature)	—	+155	—	°C	Characterized but not tested
t_{THERM}	Thermal Recovery Time (after Fault condition removed)	—	5.0	—	ms	Characterized but not tested

2.4 Timing Diagrams and Specifications

FIGURE 2-1: BUS TIMING DIAGRAM

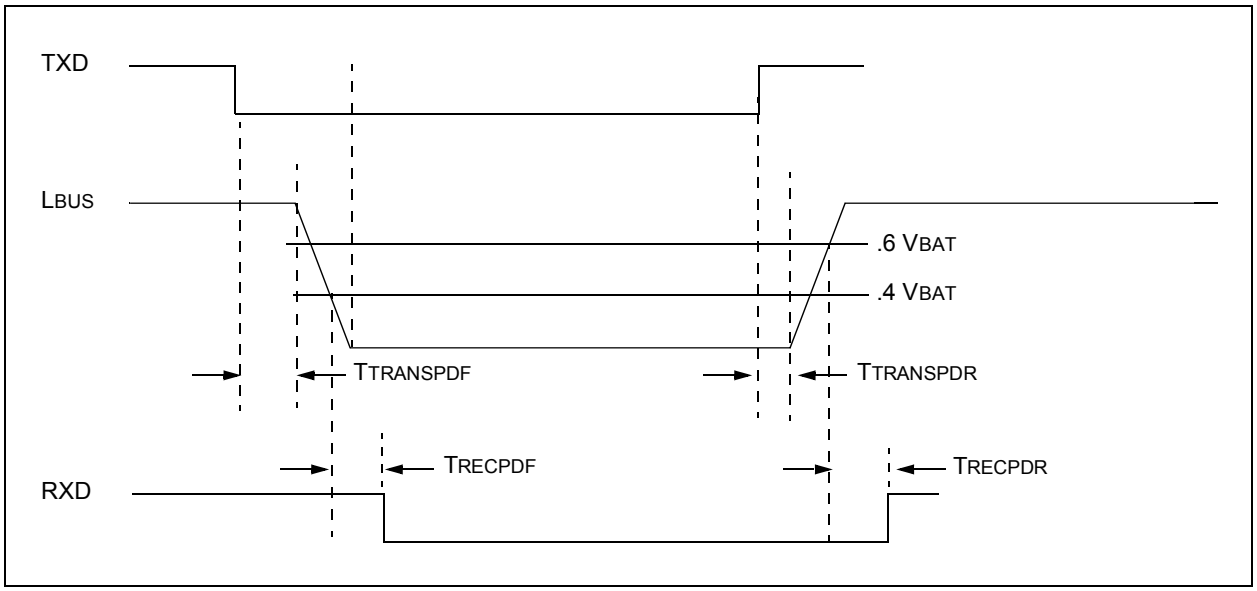


FIGURE 2-2: REGULATOR TIMING DIAGRAM ON CS/WAKE SIGNAL

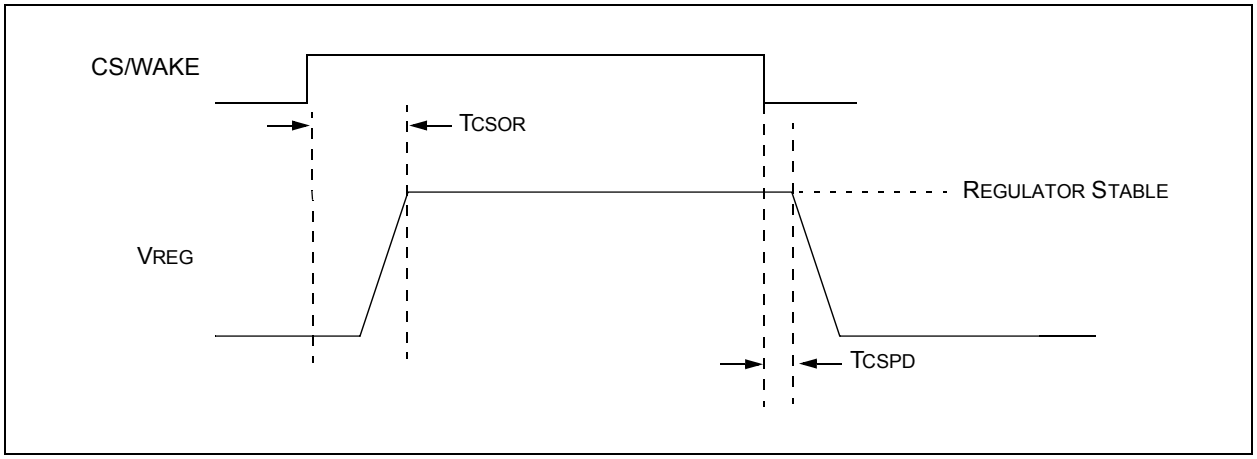


FIGURE 2-3: REGULATOR TIMING DIAGRAM ON BUS ACTIVITY

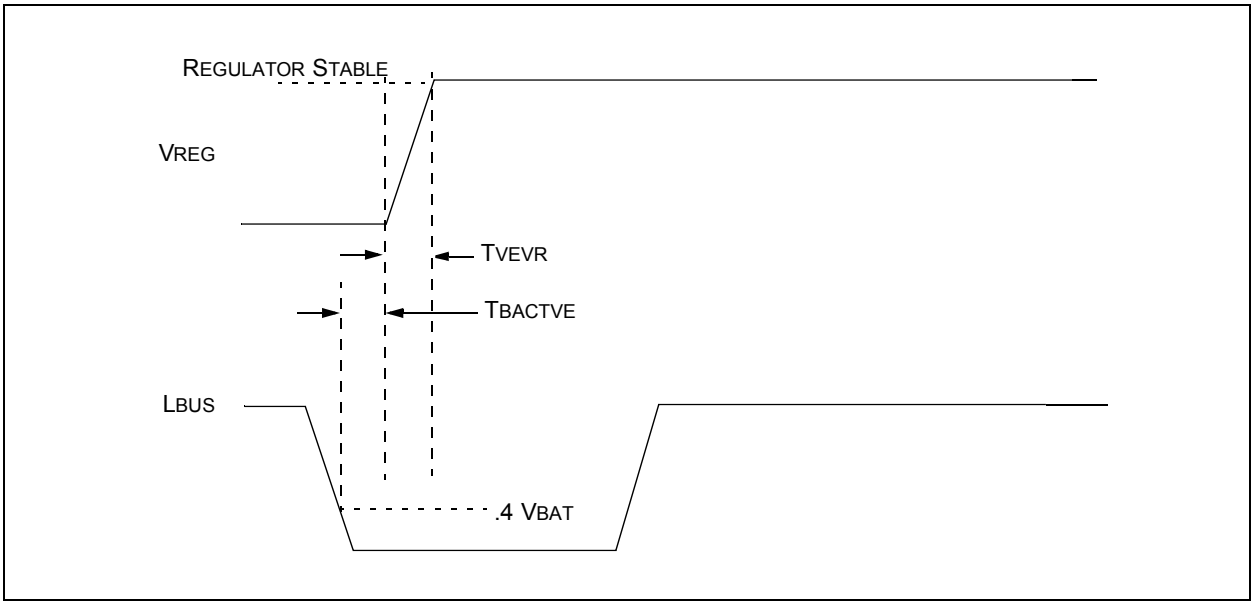
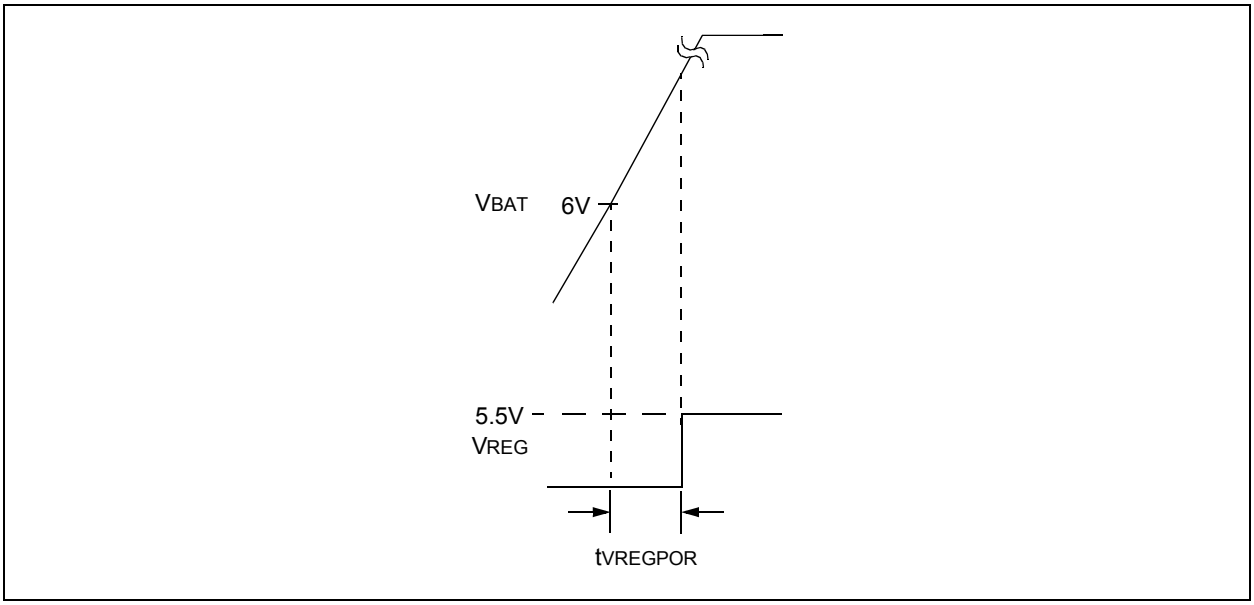


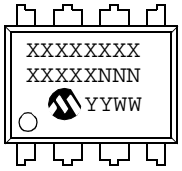
FIGURE 2-4: POR DIAGRAM



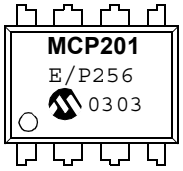
3.0 PACKAGING INFORMATION

3.1 Package Marking Information

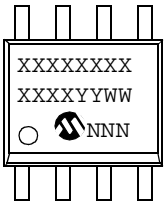
8-Lead PDIP (300 mil)



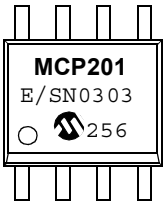
Example:



8-Lead SOIC (150 mil)



Example:

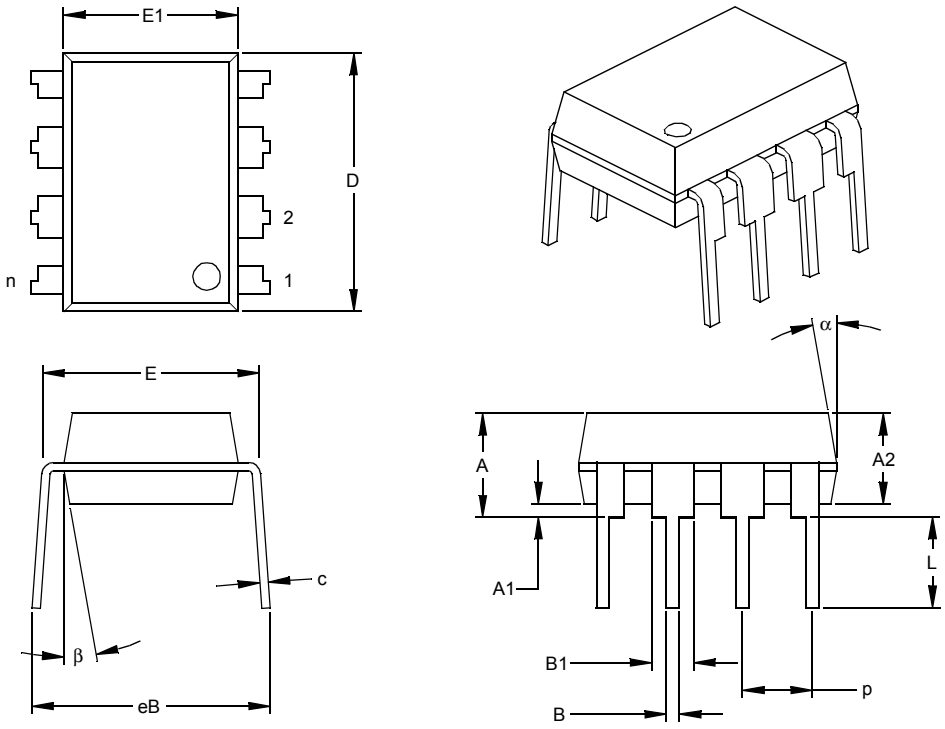


Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

***** Standard device marking consists of Microchip part number, year code, week code, and traceability code (facility code, mask rev#, and assembly code). For device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

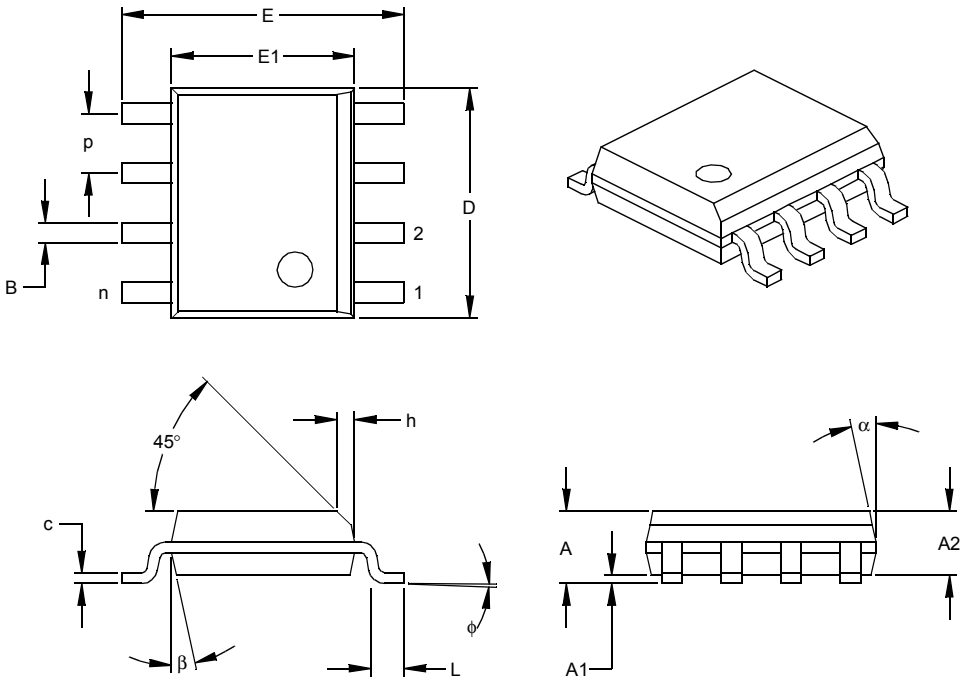


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-X	/XX
Device	Temperature Range	Package

Device:	MCP201:	LIN Transceiver with Voltage Regulator
	MCP201T:	LIN Transceiver with Voltage Regulator (Tape and Reel)
Temperature Range:	I =	-40°C to +85°C
	E =	-40°C to +125°C
Package:	P =	Plastic DIP (300 mil Body), 8-lead
	SN =	Plastic SOIC, (150 mil Body), 8-lead

Examples:

a) MCP201-E/SN: Extended Temp., SOIC package.

b) MCP201-E/P: Extended Temp., PDIP package.

c) MCP201-I/SN: Industrial Temp., SOIC package.

d) MCP201-I/P: Industrial Temp., PDIP package.

e) MCP201T-I/SN: Tape and Reel, Industrial Temp., SOIC package.

f) MCP201T-E/SN: Tape and Reel, Extended Temp., SOIC package.

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

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NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999 and Mountain View, California in March 2002. The Company's quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, non-volatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001 certified.

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