# Atmel AVR1019: Migration from ATxmega128A1/64A1 to ATxmega1281U/64A1U

## Features

- **Enhancements and added functions**
- **Reset sources**
- **I/O ports**
- **DAC – digital to analog converter**
- **AC – analog comparator**

## 1 Introduction

This application note is a guide to assist users of ATxmega128A1/64A1 in converting designs to Atmel ATxmega128A1U/64A1U. For complete device details, always refer to the most recent version of the ATxmega128A1U/64A1U datasheet and the Atmel® AVR® XMEGA® AU manual. Errata differences between ATxmega128A1/64A1 and ATxmega128A1U/64A1U are not listed in this document, only in the device datasheet.

In addition to the differences described in this document, other typical characteristics could be different. Please check the latest datasheet for details.

ATxmega128A1U/64A1U also includes new configuration options and functions. As far as possible these are implemented as a superset of existing ATxmega128A1/64A1 functions, so existing code for these devices will work on the new devices without changing existing configuration or enabling new functions. The new options and functions are listed in the application note for customers who in addition to a pure migration also wish to see an overview to consider use of the new functions.

**8-bit Atmel Microcontrollers**

**Application Note**

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# 2 Enhancements and added functions

In this section, we summarize the enhancements or added features in Atmel ATxmega128A1U/64A1U compared with Atmel ATxmega128A1/64A1. For pure migration, you can skip the section and start from the next section.

## 2.1 USB

- One USB 2.0 full speed (12Mbps) and low speed (1.5Mbps) device compliant interface is added

## 2.2 Clock system

- A divide-by-two option for the PLL output that enables output frequency down to 10MHz
- PLL lock failure detection with optionally Non-Maskable Interrupt (NMI), for improved safety and robustness
- Non-prescaled Real Time Counter clock source options: External clock from TOSC1, 32.768kHz from TOSC, and the 32.768kHz from the 32.768kHz Internal Oscillator
- The 32MHz Internal Oscillator can be tuned to run at any frequency between 30MHz and 55MHz

## 2.3 I/O ports

- Alternate pin locations for Timer/Counter 0 Compare Channels, USART0 and SPI
- Alternate pin locations for the Peripheral Clock and Event output functions

## 2.4 Analog to digital converter

- Automatic input channel scan
- VCC/2 voltage reference option
- 1/2x (divide by two) gain stage setting
- Internal ground can be used as negative input in differential mode (with gain)

## 2.5 Analog comparator

- A constant current source

## 2.6 CRC16/CRC32 generator

- A CRC16/CRC32 Generator Module that supports CRC16 (RC-CCITT) and CRC-32 (IEEE 802.3)

## 2.7 16-bit timer/counter0

- Split mode that enable two 8-bit Timer/Counters with 4PWM channels each

## 2.8 High resolution extension

- Hi-Res+ option to allow PWM resolution to be increased with 8x (3-bit)

## 2.9 Power management

- Possibility to enable sequential start of the components used for analog modules ADC and Analog Comparator in order to reduce start-up current

# 3 Reset sources

## 3.1 Brown-out detection

The programmable BODLEVEL settings are different in Atmel ATxmega128A1U/64A1U. See Table 3-1 below for details. Please refer to the device datasheet regarding tolerance for the Brown-out levels.

**Table 3-1.** Brown-out levels.

| BODLEVEL | VBOT – XMEGA AU | VBOT – XMEGA A |
|---|---|---|
| 111 | 1.6V | 1.6V |
| 110 | 1.8V | 1.9V |
| 101 | 2.0V | 2.1V |
| 011 | 2.4V | 2.6V |
| 010 | 2.6V | 2.9V |
| 000 | 3.0V | 3.4V |

## 4 I/O ports

The I/O port pins are LVTTL and LVCMOS compatible for Atmel ATxmega128A1U/64A1U devices. The minimum “Input High Voltage” is never higher than 2.0V for VCC > 2.7V.

In Atmel ATxmega128A1/64A1, the minimum “Input High Voltage” is 0.7VCC, and could be higher than 2.0V for VCC>2.86V.

# 5 DAC – digital to analog converter

The Atmel ATxmega128A1U/64A1U DAC has two continuous output channels, and not a sample and hold circuit as Atmel ATxmega128A1/64A1 devices. This gives continuous time output and higher sample rate for each channel. There is separate calibration (offset/gain) for each DAC channel in ATxmega128A1U/64A1U.

When DACA0OFFCAL (in Production Signature Row) is written to CH0OFFSETCAL in DACA, CH1OFFSETCAL is also written with this value. The details of this operation are shown below.

The first step,

- read DACA0OFFCAL from production signature row
- write DACA0OFFCAL to DACA.CH0OFFSETCAL

This will result in:

- DACA.CH0OFFSETCAL = DACA0OFFCAL
- DACA.CH1OFFSETCAL = DACA0OFFCAL

The second step,

- read DACA1OFFCAL from production signature row
- write DACA1OFFCAL to DACA.CH1OFFSETCAL

This will result in:

- DACA.CH1OFFSETCAL = DACA1OFFCAL

After that, any further writing to DACA.CH0OFFSELCAL does not change DACA.CH1OFFSELCAL until the next reset. The same is implemented for both OFFSET and GAIN calibration registers in DACA and DACB. This ensure that customers using the ATxmega128A1/64A1 DAC can continue and use the same calibration sequence and still calibrate both channels.

TIMCTRL register does not exist in ATxmega128A1U/64A1U, so there are no timing constraints on DAC operation.

## 6 AC – analog comparator

In Atmel ATxmega128A1U/64A1U, there is a two-cycle delay from writing a new MUX setting until it takes effect.

# 7 Registers

## 7.1 Removed registers and bits

The below table lists register bits, which exist in Atmel ATxmega128A1/64A1 but not in Atmel ATxmega128A1U/64A1U.

**Table 7-1.** Register bits and functionality that does not exist in ATxmega128A1U/64A1U.

| Register name | Register bit | Function |
|---|---|---|
| FUSEBYTE2 | BODACT[1:0](1) | BOD functionality when in active mode |
| TIMCTRL | CONINTVAL[2:0] | DAC Conversion Interval |
| | REFRESH[3:0] | DAC Channel Refresh Timing Control |

Note: 1. BODACT fuses are now located in FUSEBYTE5 for all devices.

# 8 Table of contents

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