Errata

- **Increased Interrupt Latency**
- **Interrupts Abort TWI Power-down**
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6. Increased Interrupt Latency

In this device, some instructions are not interruptable, and will cause the interrupt latency to increase. The only practical problem concerns a loop followed by a two-word instruction while waiting for an interrupt. The loop may consist of a branch instruction or an absolute or relative jump back to itself like this:

```
loop: rjmp loop
<Two-word instruction>
```

In this case, a dead-lock situation arises.

Problem Fix/Workaround

In assembly, insert a nop instruction immediately after a loop to itself. The problem will normally be detected during development. In C, the only construct that will give this problem is an empty “for” loop; “for(;;)”. Use “while(1)” or “do{} while (1)” to avoid the problem.

5. Interrupts Abort TWI Power-down

TWI power-down operation may be aborted by other interrupts. If an interrupt (e.g. INT0) occurs during TWI power-down address watch and wakes the CPU up, the TWI aborts operation and returns to its idle state.

Problem Fix/Workaround

Ensure that the TWI Address Match is the only enabled interrupt when entering power-down.

4. TWI Master Does not Accept Spikes on Bus Lines

When the part operates as master, and the bus is idle (SDA = 1; SCL = 1), generating a short spike on SDA (SDA = 0 for a short interval), no interrupt is generated, and the status code is still $F8 (idle). But when the software initiates a new start condition and clears TWINT, nothing happens on SDA or SCL, and TWINT is never set again.

Problem Fix/Workaround

Either of the following:

1. Ensure that no spikes occur on SDA or SCL lines.
2. Receiving a valid START condition followed by a STOP condition provokes a bus error reported as a TWI interrupt with status code $00.
3. In a single master systems, the user should write the TWSTO bit immediately before writing the TWSTA bit.

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3. TWCR Write Operation Ignored

Repeated write to TWCR must be delayed. If a write operation to TWCR is immediately followed by another write operation to TWCR, the first write operation may be ignored.

Problem Fix/Workaround

Ensure at least one instruction (e.g., nop) is executed between two writes to TWCR.

2. PWM not Phase Correct

In Phase-correct PWM mode, a change from OCRx = TOP to anything less than TOP does not change the OCx output. This gives a phase error in the following period.

Problem Fix/Workaround

Make sure this issue is not harmful to the application.

1. TWI is Speed Limited in Slave Mode

When the 2-wire Serial Interface operates in slave mode, frames may be undetected if the CPU frequency is less than 64 times the bus frequency.

Problem Fix/Workaround

Ensure that the CPU frequency is at least 64 times the TWI bus frequency.

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