
Errata

- Interrupts Abort TWI Power-down
- TWI Master Does not Accept Spikes on Bus Lines
- TWCR Write Operations Ignored when Immediately Repeated
- PWM not Phase Correct
- TWI is Speed Limited in Slave Mode
- Problems with UBRR Settings
- Missing Overrun Flag and Fake Frame Error in USART

7. Interrupts Abort TWI Power-down

TWI Power-down operation may wake up by other interrupts. If an interrupt (e.g. INTO) occurs during TWI Power-down address watch and wakes up the CPU, the TWI aborts operation and returns to its idle state.

If the interrupt occurs in the middle of a Power-down address match (i.e., during reading of a slave address), the received address will be lost and the slave will not return an ACN

Problem Fix/Workaround

Ensure that the TWI Address Match is the only enabled interrupt when entering Power-down.

The master can handle this by resending the request if NACK is received.

6. TWI Master Does not Accept Spikes on Bus Lines

When the part operates as master, and the bus is idle (SDA = 1; SCL = 1), generating a short spike on SDA (SDA = 0 for a short interval), no interrupt is generated, and the status code is still \$F8 (idle). But when the software initiates a new start condition and clears TWINT, nothing happens on SDA or SCL, and TWINT is never set again.

Problem Fix/Workaround

Either of the following:

1. Ensure no spikes occur on SDA or SCL lines.
2. Generate a valid START condition followed by a STOP condition on the bus. This provokes a bus error reported as a TWI interrupt with status code \$00.
3. In a single-master system, the user should write the TWSTO bit immediately before writing the TWSTA bit.

5. TWCR Write Operation Ignored when Immediately Repeated

Repeated write to TWCR must be delayed. If a write operation to TWCR is immediately followed by another write operation to TWCR, the first write operation may be ignored.

Problem Fix/Workaround

Ensure at least one instruction (e.g., NOP) is executed between two writes to TWCR.



8-bit AVR[®]
Microcontroller
with 32K Bytes
In-System
Programmable
Flash

ATmega323(L)
Rev. B
Errata Sheet

Rev. 2497A-10/01



4. PWM not Phase Correct

In Phase-correct PWM mode, a change from OCRx = TOP to anything less than TOP does not change the OCx output. This gives a phase error in the following period.

Problem Fix/Workaround

Make sure this issue is not harmful to the application.

3. TWI is Speed Limited in Slave Mode

When the 2-wire Serial Interface operates in Slave mode, frames may be undetected if the CPU frequency is less than 64 times the bus frequency.

Problem Fix/Workaround

Ensure that the CPU frequency is at least 64 times the TWI bus frequency.

2. Problems with UBRR Settings

The baud rate corresponding to the previous UBRR setting is used for the first transmitted/received bit when either UBRRH or UBRRL is written. This will disturb communication if the UBRR is changed from a very high to a very low baud rate setting, as the internal baud rate counter will have to count down to zero before using the new setting.

In addition, writing to UBRRL incorrectly clears the UBRRH setting.

Problem Fix/Workaround

UBRRH must be written after UBRRL because setting UBRRL clears UBRRH. By doing an additional dummy write to UBRRH, the baud rate is set correctly. The following is an example on how to set UBRR. UBRRH is updated first for upward compability with corrected devices.

```
ldi r17, HIGH(baud)
ldi r16, LOW(baud)
out UBRRH, r17      ; Added for upward compability
out UBRRL, r16      ; Set new UBRRL, UBRRH incorrectly cleared
out UBRRH, r17      ; Set new UBRRH
out UBRRH, r17      ; Loads the baud rate counter with new (correct) value
```

1. Missing Overrun Flag and Fake Frame Error in USART

When the USART has received three characters without any of them been read, the USART FIFO is full. If the USART detects the start bit of a fourth character, the Data Overrun (DOR) Flag will be set for the third character. However, if a read from the USART Data Register is performed just after the start bit of the fourth byte is received, a frame error is generated for character three. If the USART Data Register is read between the reception of the first data bit and the end of the fourth character, the Data Overrun Flag of character three will be lost.

Problem Fix/Workaround

The user should design the application to never completely fill the USART FIFO. If this is not possible, the user must use a high-level protocol to be able able to detect if any characters were lost and request a retransmission if this happens.



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