E-LAB Technical-Informations

Computers

What is JTAG?

JTAG (abbr. of Joint Test Access Group) is a test and programming interface for digital IC's used by over 200 electronic companies. Intentional designed for programmable logic chips (IEEE 1149.1) it is now widely used as a standard in the microcontroller market.

Since the introduction of the Mega323 and Mega 128 also Atmel has implemented the 4 wire (TMS, TCK, TDI, TDO) serial protocol in the new CPUs.

The JTAG–unit can be seen as a large shift register through the entire IC where each bit (Ports, RAM, Register etc.) can be accessed like a conveyor belt in a parcel distribution.

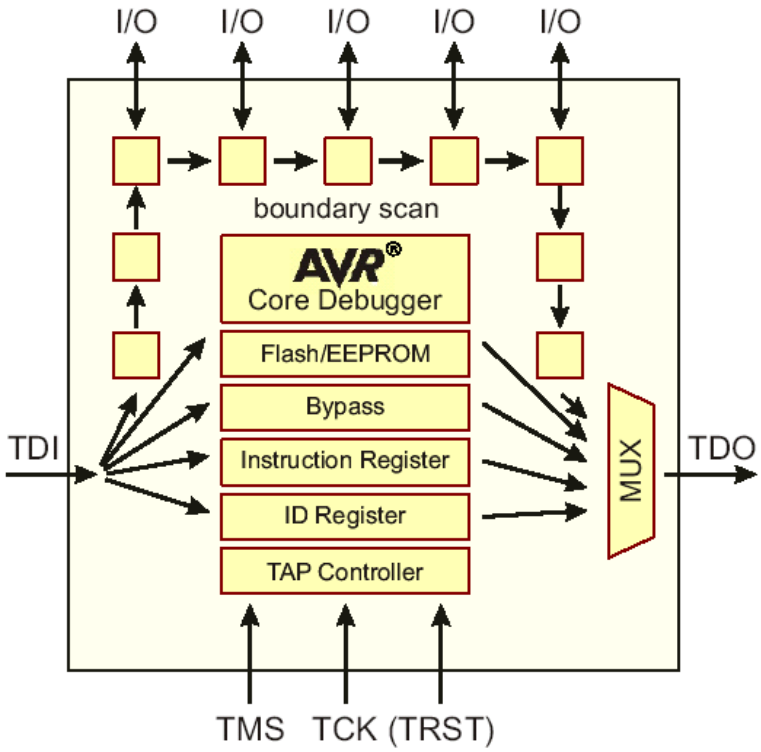
Atmel stated that each upcoming AVR with at least 16 kBytes Flash (eg. the Mega16) will support JTAG.

A reverse engineering of protected software is still disabled because the lockbits also work in JTAG mode. But also the complete JTAG interface can be disabled after programming. With the JTAG interface the Flash an EEprom memory of the AVR can be in-system programmed in high speed. In addition nearly each peripheral unit of the controller easily can be accessed, tested and debugged.

The programming of the Flash/EEprom is not dependent of the CPU's clock frequency like the convential SPI programming. This means that the AVR doesn't need a working clock hardware (internal or external) for programming with the maximal speed. So the programming time is mostly dependent of the time a cell or block needs for programming itself.

The debugging via JTAG implements error detection in firmware with the help of the *origin CPU* and not with the probe of an ICE-Emulators. This gives much more relistic results. The JTAG circuit in the AVR supports hardware- and software breakpoints of different kind. The CPU can be stopped or single stepped in a similar way like a $xxxx emulator but much more *cheaper*.

E-LAB-Computers implements the JTAG interface into all present and new programmer devices (ICP-V24/USB, ICPII-V24/USB and ISP-V24/USB).



The programming of the CPUs via JTAG is already implemented in the newest devices. Somewhat later the debugger of our AVRco-Pascal-Compiler Profi version will support the direct debugging of apps in the target CPU. The programmer then serves as a JTAG-to-PC-adaptor.

Also in the future there will be an option to design own test programs for a simple way of In-Circuit-Test. This gives the small and medium series hardware producers a cheap, simple and flexible testing of complete boards.

So look forward to faster in-system programming and cheaper and userfriendly debugging in the well known E-LAB quality.

The JTAG connector pin assignment of the E-LAB programmers