SPI/I²C® Compatible, 10-Bit Digital Temperature Sensor and Eight Channel ADC

Preliminary Technical Data — ADT7411

FEATURES

10-Bit Temperature to Digital Converter
10-Bit Eight Channel ADC :
DC Input Bandwidth
Input Range: 0 V to 2.25 V and 0 V to V_{DD}
Temperature range: -40°C to +125°C
Temperature Sensor Accuracy of ±0.5°C
Supply Range : + 2.7 V to + 5.5 V

Power-Down Current 1µA
Internal 2.25 V_{Ref} Option
Double-Buffered Input Logic
Buffered / Unbuffered Reference Input Option

I²C®, SPI™, QSPI™, MICROWIRE™ and DSP-Compatible 4-wire Serial Interface
16-Lead QSOP Package

APPLICATIONS

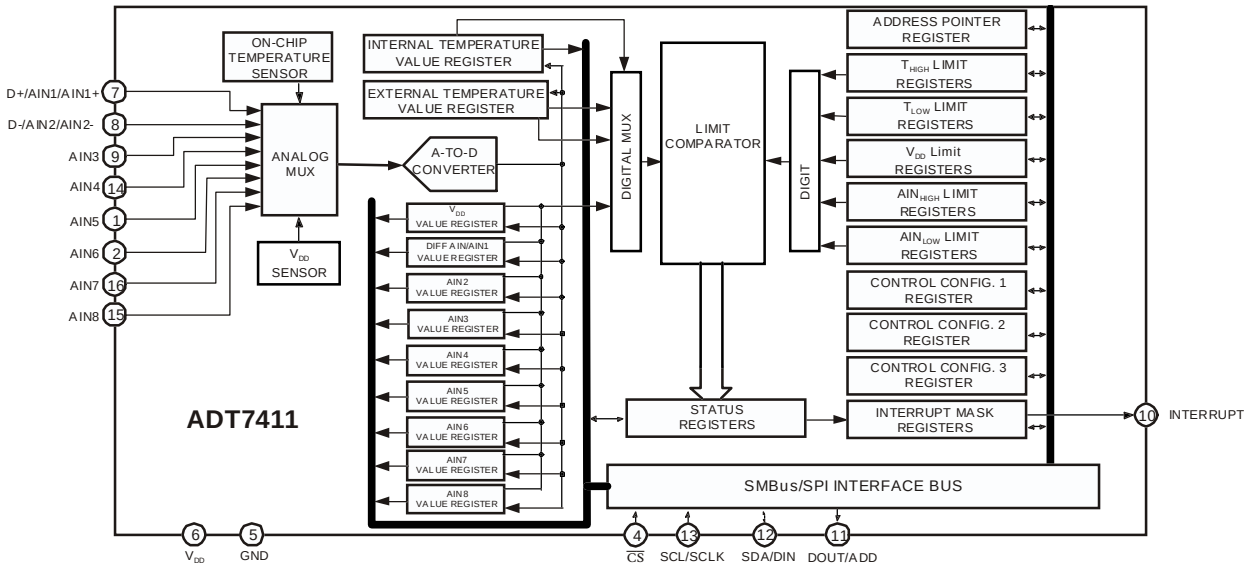
Portable Battery Powered Instruments
Personal Computers
Smart Battery Chargers
Telecommunications Systems
Electronic Test Equipment
Domestic Appliances
Process Control

GENERAL DESCRIPTION

The ADT7411 combines a 10-Bit Temperature-to-Digital Converter and a 10-Bit Eight Channel ADC, in a 16-Lead QSOP package. This includes a bandgap temperature sensor and a 10-bit ADC to monitor and digitize the temperature reading to a resolution of 0.25 °C. The ADT7411 operates from a single +2.7 V to + 5.5 V supply. The input voltage range on the ADC channels has a range of 0V to 2.25V and the input bandwidth is DC. The reference for the ADC channels is derived internally. The ADT7411 provides two serial interface options, a four-wire serial interface which is compatible with SPI™, QSPI™, MICROWIRE™ and DSP interface standards; and a two-wire I²C interface. It features a standby mode that is controlled via the serial interface.

The ADT7411's wide supply voltage range, low supply current and SPI/I²C-compatible interface, make it ideal for a variety of applications, including personal computers, office equipment and domestic appliances.

FUNCTIONAL BLOCK DIAGRAM



REV. PrE 02/'02

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ADT7411-SPECIFICATIONS[1]

(V_{DD}=2.7 V to 5.5 V, GND=0 V, unless otherwise noted)

Parameter[2]	Min	Typ	Max	Units	Conditions/Comments
ADC DC ACCURACY					
Resolution			10	Bits	
Integral Nonlinearity			±2	LSB	
Differential Nonlinearity			±0.9	LSB	
Offset Error			±2	% of FSR	
Offset Error Match			±0.5	LSB	
Gain Error			±2	% of FSR	
Gain Error Match			±0.5	LSB	
ADC Bandwidth			DC	Hz	
ANALOG SINGLE ENDED INPUTS					
Input Voltage Range	0		2.25	V	AIN1 to AIN8. C4 = 0 in Control Config. 3.
	0		V_{DD}	V	AIN1 to AIN8. C4 = 1 in Control Config. 3.
DC Leakage Current			±1	µA	
Input Capacitance		tbd	tbd	pF	
ANALOG SINGLE DIFFERENTIAL INPUTS					
Full Scale Input Span			65	mV	AIN1+ to AIN2-.
Absolute Input Voltage					
AIN1+	0		V_{DD}-V_{DIFF}Max	V	V_{DIFF}Max = 65 mV.
AIN2-	0		V_{DD}-V_{DIFF}Max	V	
Full Scale Accuracy			±2	% of FSR	
THERMAL CHARACTERISTICS INTERNAL TEMPERATURE SENSOR					Internal Reference used.
Accuracy @ V_{DD}=3.3V			±2	°C	T_A = 0°C to +85°C
			±3	°C	T_A = -40°C to +125°C
Accuracy @ V_{DD}=5V		±2		°C	T_A = 0°C to +85°C
		±3		°C	T_A = -40°C to +125°C
Resolution			10	Bits	
Long Term Drift		0.5		°C/1000hrs	
EXTERNAL TEMPERATURE SENSOR					External Transistor = 2N3906.
Accuracy @ V_{DD}=3.3V			±2	°C	T_A = 0°C to +85°C.
			±3	°C	T_A = -40°C to +125°C
Accuracy @ V_{DD}=5V		±2		°C	T_A = 0°C to +85°C
		±3		°C	T_A = -40°C to +125°C
Resolution			10	Bits	
Update Rate, t_R		400		µs	Round Robin[5] enabled
		50		µs	Round Robin disabled
Temperature Conversion Time		25		µs	
Output Source Current		180		µA	High Level
		11		µA	Low Level
ON-CHIP REFERENCE					
Reference Voltage[3]		2.25		V	
Temperature Coefficient[3]		80		ppm/°C	
DIGITAL INPUTS[3]					
Input Current			±1	µA	V_{IN} = 0V to V_{DD}
V_{IL}, Input Low Voltage			0.8	V	V_{DD} = +5V±10%
			0.6	V	V_{DD} = +3V±10%
V_{IH}, Input High Voltage	1.89			V	
Pin Capacitance		3	10	pF	All Digital Inputs
SCL, SDA Glitch Rejection			50	ns	Input Filtering Suppresses Noise Spikes of Less than 50 ns
DIGITAL OUTPUT					

Parameter[2]	Min	Typ	Max	Units	Conditions/Comments
Output High Voltage, V_{OH}	2.4			V	$I_{SOURCE} = I_{SINK} = 200\ \mu A$
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 3 mA
Output High Current, I_{OH}			1	mA	V_{OH} = 5 V
Output Capacitance, C_{OUT}			50	pF	
INTERRUPT Output Saturation Voltage			0.8	V	I_{OUT} = 4 mA
I²C TIMING CHARACTERISTICS[4,5]					
Serial Clock Period, t_1	2.5			µs	Fast-Mode I²C. See Figure 1
Data In Setup Time to SCL High, t_2					
Data Out Stable after SCL Low, t_3	0			ns	See Figure 1
SDA Low Setup Time to SCL Low (Start Condition), t_4	50			ns	See Figure 1
SDA High Hold Time after SCL High (Stop Condition), t_5	50			ns	See Figure 1
SDA and SCL Fall Time, t_6			90	ns	See Figure 1
SPI TIMING CHARACTERISTICS[6,7]					
$\overline{CS}$ to SCLK Setup Time, t_1	0			ns	See Figure 2
SCLK High Pulsewidth, t_2	50			ns	See Figure 2
SCLK Low Pulse, t_3	50			ns	See Figure 2
Data Access Time after SCLK Falling edge, t_4[8]			35	ns	See Figure 2
Data Setup Time Prior to SCLK Rising Edge, t_5	20			ns	See Figure 2
Data Hold Time after SCLK Rising Edge, t_6	0			ns	See Figure 2
$\overline{CS}$ to SCLK Hold Time, t_7	0			ns	See Figure 2
$\overline{CS}$ to DOUT High Impedance, t_8			40	ns	See Figure 2
POWER REQUIREMENTS					
V_{DD}	2.7		5.5	V	
V_{DD} Settling Time			50	ms	V_{DD} settles to within 10% of it's final voltage level
I_{DD} (Normal Mode)[9]	0.85		1.3	mA	$V_{IH} = V_{DD}$ and V_{IL} = GND
I_{DD} (Power Down Mode)	1		3	µA	V_{DD} = +4.5V to +5.5V, $V_{IH}=V_{DD}$ and V_{IL}=GND
	0.5		1	µA	V_{DD} = +2.7V to +3.6V, $V_{IH}=V_{DD}$ and V_{IL}=GND
Power Dissipation	tbd	tbd	tbd	µW	V_{DD} = +2.7 V. Using Normal Mode
	tbd	tbd	tbd	µW	V_{DD} = +2.7 V. Using Shutdown Mode

Notes:
[1] Temperature ranges are as follows: A Version: -40°C to +125°C.
[2] See Terminology.
[3] Guaranteed by Design and Characterization, not production tested
[4] The SDA & SCL timing is measured with the input filters turned on so as to meet the Fast-Mode I²C specification. Switching off the input filters improves the transfer rate but has a negative affect on the EMC behaviour of the part.
[5] Guaranteed by design. Not tested in production.
[6] Guaranteed by design and characterization, not production tested.
[7] All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.
[8] Measured with the load circuit of Figure 3.
[9] I_{DD} spec. is valid for fullscale analog input voltages. Interface inactive. ADC active. Load currents excluded.
Specifications subject to change without notice.

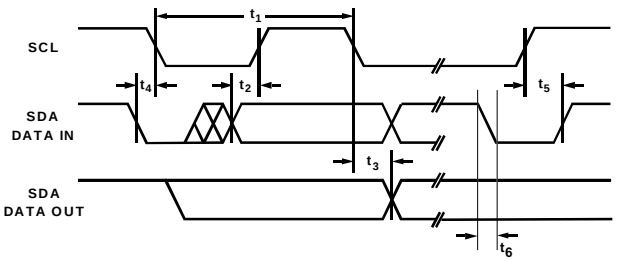


Figure 1. Diagram for I²C Bus Timing

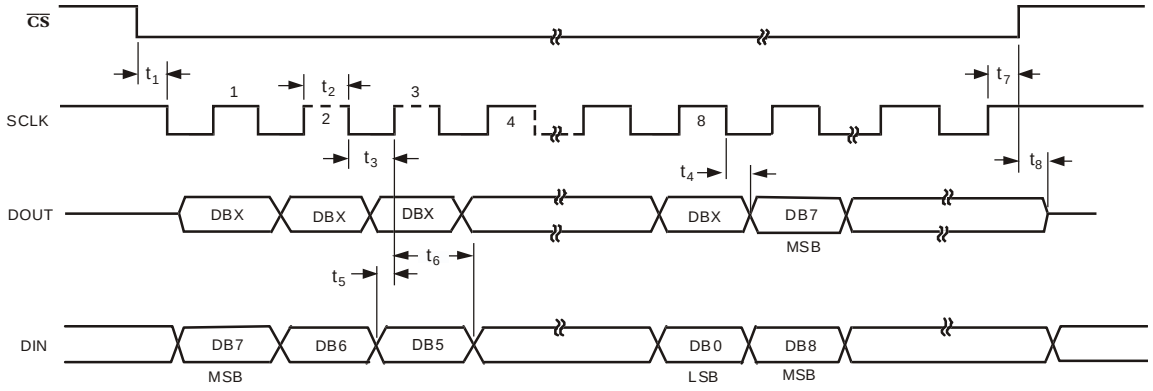


Figure 2. Diagram for SPI Bus Timing

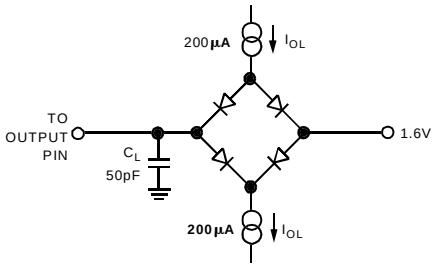


Figure 3. Load Circuit for Access Time and Bus Relinquish Time

ABSOLUTE MAXIMUM RATINGS*

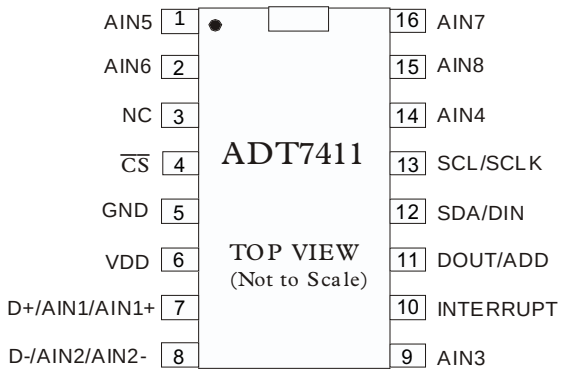
V_{DD} to GND	–0.3 V to +7 V
Analog Input Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	+150°C
16-Lead QSOP Package	
Power Dissipation	(T_j max - T_A) / θ_{JA}
θ_{JA} Thermal Impedance	150 °C/W (QSOP)
Reflow Soldering	
Peak Temperature	+220 +/- 0°C
Time of Peak Temperature	10 sec to 40 sec

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 1. I^2C Address Selection

ADD Pin	I^2C Address
Low	1001 000
Float	1001 010
High	1001 011

PIN CONFIGURATION
QSOP



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
ADT7411ARQ	–40°C to +125°C	16-Lead QSOP	RQ-16

CAUTION
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADT7411 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ADT7411 PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	AIN5	Analog input. Single ended analog input channel. Input range is 0 V to 2.25 V or 0 V to V_{DD}.
2	AIN6	Analog input. Single ended analog input channel. Input range is 0 V to 2.25 V or 0 V to V_{DD}.
3	NC	No connection to this pin.
4	$\overline{CS}$	SPI Active low control Input. This is the frame synchronization signal for the input data. When CS goes low, it enables the input register and data is transferred in and out on the rising edges of the following serial clocks. This pin must be kept high for I^2C mode of operation. $\overline{CS}$ is also used as a control pin when selecting the serial interface type after power-up.
5	GND	Ground Reference Point for All Circuitry on the part. Analog and Digital Ground.
6	V_{DD}	Positive Supply Voltage, +2.7 V to +5.5 V.The supply should be decoupled to ground.
7	D+/AIN1/AIN1+	D+. Positive connection to external temperature sensor. AIN1. Analog Input. Single ended analog input channel. Input range is 0 V to 2.25 V or 0 V to V_{DD}. AIN1+. Analog Input. Positive differential ended analog channel. Input range is 0 V to 65 mV.
8	D-/AIN2/AIN2-	D-. Negative connection to external temperature sensor. AIN2. Analog Input. Single ended analog input channel. Input range is 0 V to 2.25 V or 0 V to V_{DD}. AIN2-. Analog Input. Negative differential ended analog channel. Input range is 0 V to 65 mV.
9	AIN3	Analog input. Single ended analog input channel. Input range is 0 V to 2.25 V or 0 V to V_{DD}.
10	INTERRUPT	Over Limit Interrupt. The output polarity of this pin can be set to give an active low or active high interrupt when temperature, V_{DD} and AIN limits are exceeded. Default is active low.
11	DOUT/ADD	SPI Serial Data Output. Logic Output. Data is clocked out of any register at this pin. Data is clocked out on the falling edge of SCLK. ADD. I^2C serial bus address selection pin. Logic input. During the first valid I^2C bus communication this pin is checked to determine the serial bus address assigned to the ADT7411. Any subsequent changes on this pin will have no affect on the I^2C serial bus address. A low on this pin gives the address 1001 000, leaving it floating gives the address 1001 010 and setting it high gives the address 1001 011.
12	SDA/DIN	SDA. I^2C Serial Data Input. I^2C serial data to be loaded into the parts registers is provided on this input. DIN. SPI Serial Data Input. Serial data to be loaded into the parts registers is provided on this input. Data is clocked into a register on the rising edge of SCLK.
13	SCL/SCLK	Serial Clock Input. This is the clock input for the serial port. The serial clock is used to clock data out of any register of the ADT7411 and also to clock data into any register that can be written to.
14	AIN4	Analog input. Single ended analog input channel. Input range is 0 V to 2.25 V or 0 V to V_{DD}.
15	AIN8	Analog input. Single ended analog input channel. Input range is 0 V to 2.25 V or 0 V to V_{DD}.
16	AIN7	Analog input. Single ended analog input channel. Input range is 0 V to 2.25 V or 0 V to V_{DD}.

TERMINOLOGY

RELATIVE ACCURACY

Relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the ADC transfer function.

DIFFERENTIAL NONLINEARITY

Differential Nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. The ADC is guaranteed monotonic by design.

OFFSET ERROR

This is a measure of the offset error of the ADC. It can be negative or positive. It is expressed in mV.

OFFSET ERROR MATCH

This is the difference in Offset Error between any two channels

GAIN ERROR

This is a measure of the span error of the ADC. It is the deviation in slope of the actual ADC transfer characteristic from the ideal expressed as a percentage of the full-scale range.

GAIN ERROR MATCH

This is the difference in Gain error between any two channels.

OFFSET ERROR DRIFT

This is a measure of the change in offset error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

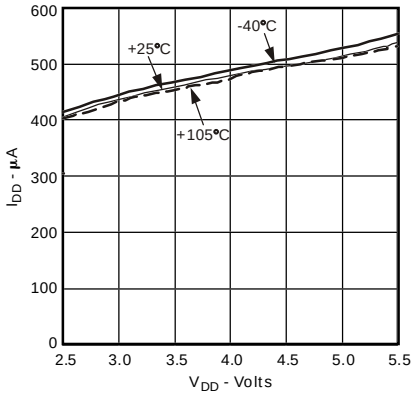
GAIN ERROR DRIFT

This is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

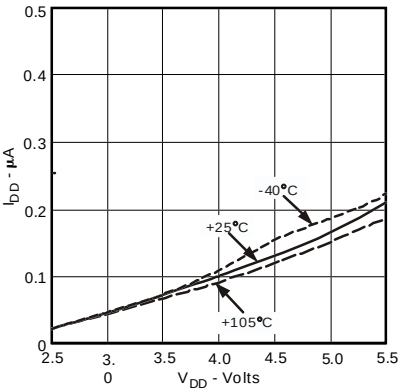
DC POWER-SUPPLY REJECTION RATIO (PSRR)

ROUND ROBIN

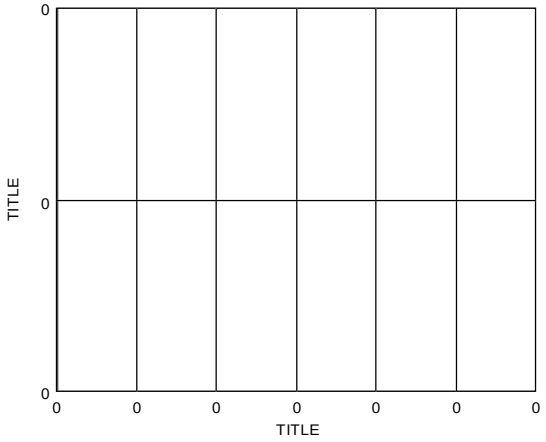
This term is used to describe the ADT7411 cycling through the available measurement channels in sequence, taking a measurement on each channel.



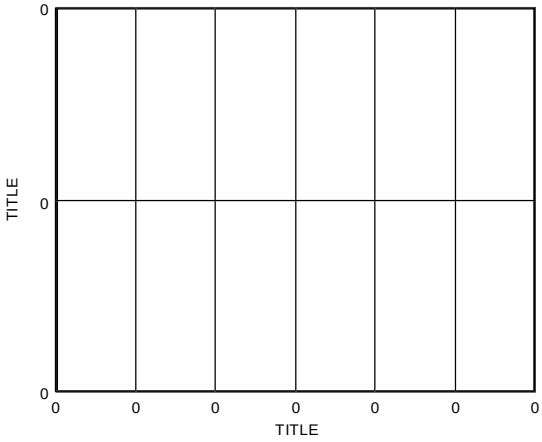
TPC 1. Supply Current vs. Supply Voltage



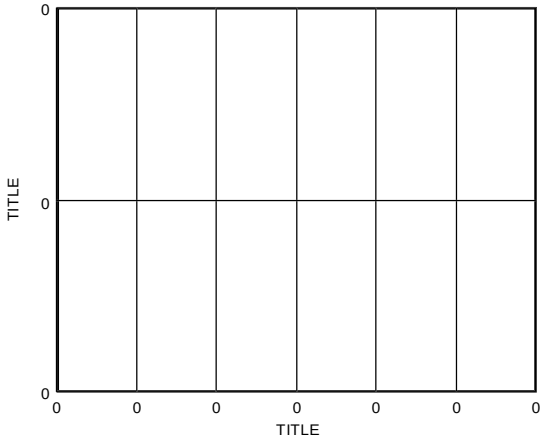
TPC 2. Power-Down Current vs. Supply Voltage



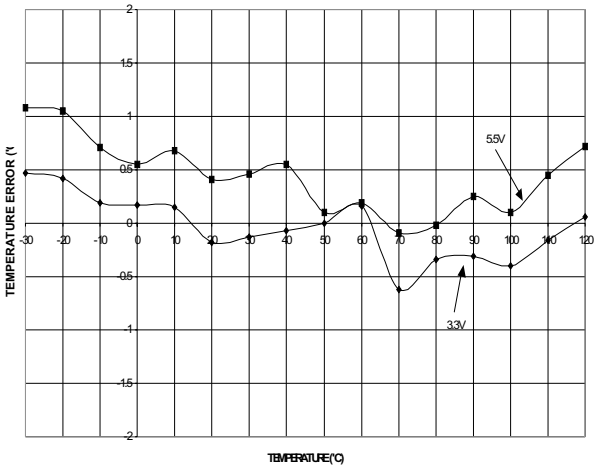
TPC 3. ADC DNL



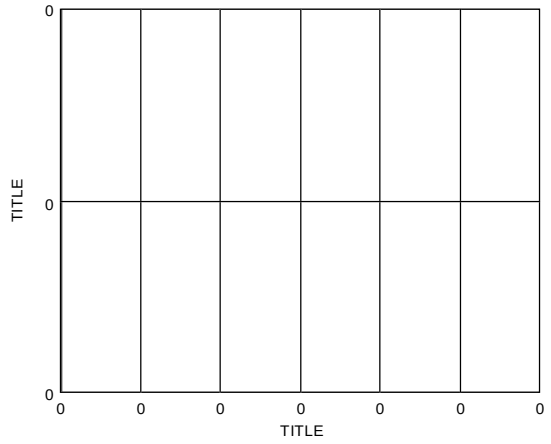
TPC 4. ADC INL



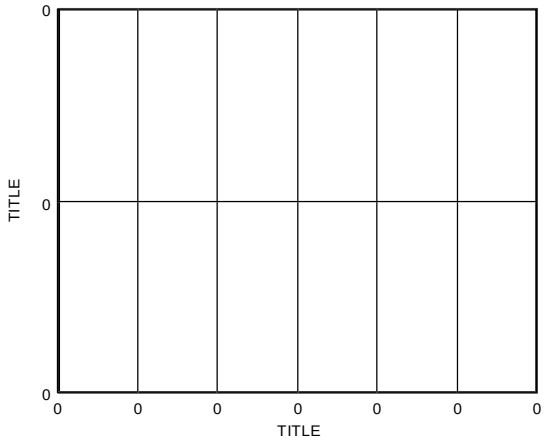
TPC 5. PSRR vs Supply Ripple Frequency



TPC 6. Temperature Error @ 3.3 V and 5 V



TPC 7. ADC Offset Error and Gain Error vs Temperature



TPC 8. ADC Offset Error and Gain Error vs V_{DD}

FUNCTIONAL DESCRIPTION - ANALOG INPUTS

SINGLE-ENDED INPUTS

The ADT7411 offers eight single-ended analog input channels. The analog input range is between 0 V to 2.25 V or 0 V to V_{DD}. Selection between the two input ranges is done by Bit C4 of Control Congifuration 3 Register (Address = 1Ah). Setting this bit to 0 sets up the analog input ADC reference to be sourced from the internal voltage reference of 2.25 V. Setting the bit to 1 sets up the ADC reference to be sourced from V_{DD}.

The ADC resolution is 10 bits and is mostly suitable for DC input signals or very slow varying AC signals. Bits C1:2 of Control Configuration 1 register (Address = 18h) are used to set up AIN1 and AIN2 as either single-ended inputs or as a differential-ended input. The default setting on power-up is for AIN1 and AIN2 to be single-ended inputs. Figure 4 shows the overall view of the four channel analog input path.

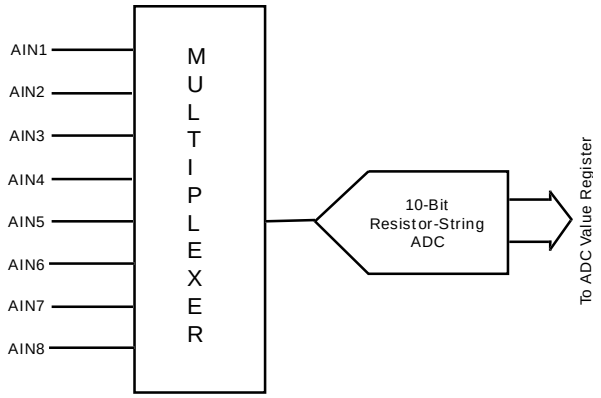


Figure 4. Quad Single-Ended Analog Input Path

CONVERTER OPERATION

The analog input channels use a successive approximation ADC based around a resistor-string DAC. Figures 5 and 6 show simplified schematics of the ADC. Figure 5 shows the ADC during acquisition phase. SW2 is closed and SW1 is in position A. The comparator is held in a balanced condition and the sampling capacitor acquires the signal on AIN.

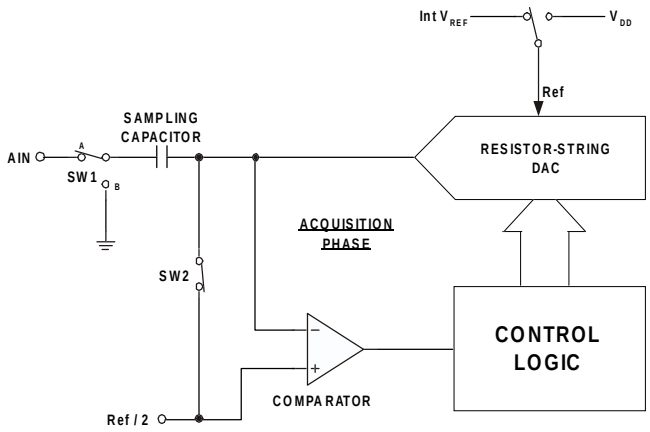


Figure 5. ADC Acquisition Phase

When the ADC eventually goes into conversion phase, see Figure 6, SW2 opens and SW1 moves to position B causing the comparator to become unbalanced. The control logic and the DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced the conversion is complete. The control logic generates the ADC output code. Figure 8 shows the ADC transfer function for single-ended analog inputs.

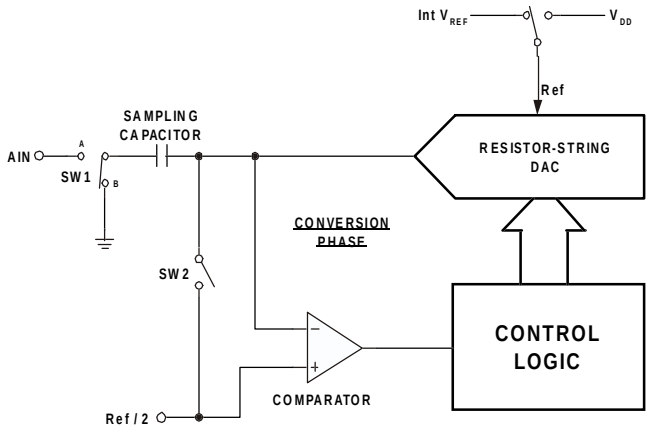


Figure 6. ADC Conversion Phase

ADC SINGLE-ENDED TRANSFER FUNCTION

The output coding of the ADT7411 single-ended analog inputs is straight binary. The designed code transitions occur midway between successive integer LSB values (i.e. 1/2LSB, 3/2LSB, etc.). The LSB is $V_{DD}/1024$ or Int $V_{REF}/1024$, Int V_{REF} = 2.25 V. The ideal transfer characteristic is shown in figure 8 below.

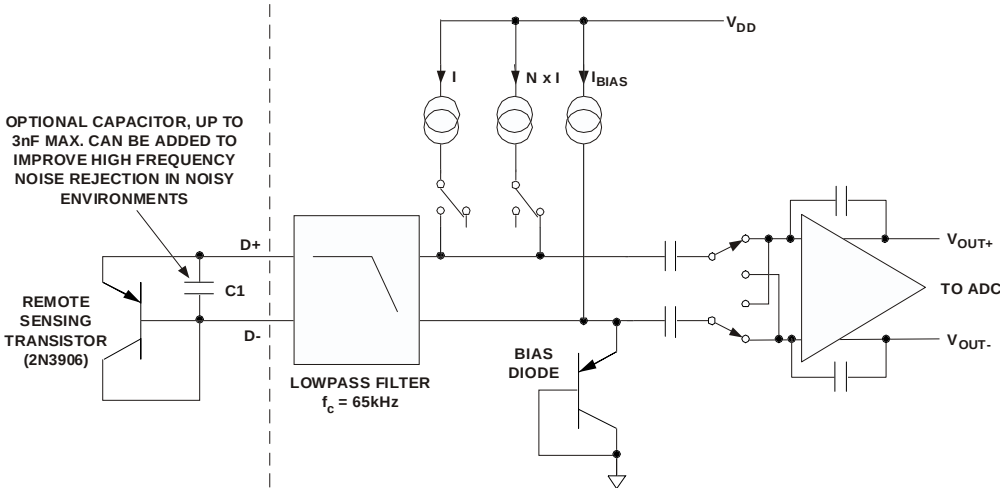


Figure 7. Signal Conditioning for External Diode Temperature Sensor

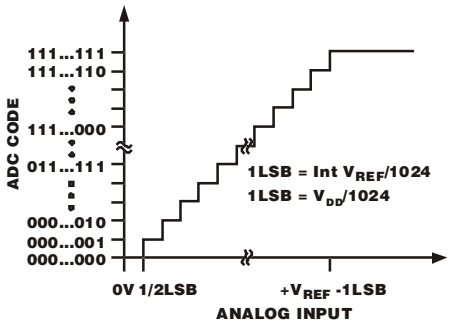


Figure 8. Single-Ended Transfer Function

ANALOG INPUT ESD PROTECTION

Figure 9 shows the input structure on any of the analog input pins that provides ESD protection. The diode provides the main ESD protection for the analog inputs. Care must be taken that the analog input signal never drops below the GND rail by more than 200mV. If this happens then the diode will become forward biased and start conducting current into the substrate. The 4pF capacitor is the typical pin capacitance and the resistor is a lumped component made up of the on-resistance of the multiplexer switch.

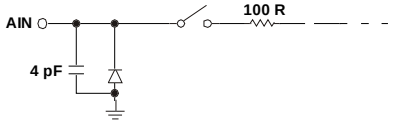


Figure 9. Equivalent Analog Input ESD Circuit

DIFFERENTIAL ENDED INPUTS

The ADT7411 offers one differential-ended analog input channel. This channel uses the AIN1 and AIN2 inputs as AIN1+ and AIN2- respectively. The analog input span is between 0 V to 65 mV.

The ADC resolution is 10 bits and is mostly suitable for DC input signals or very slow varying AC signals. Bits C1:2 of Control Configuration 1 register (Address = 18h) are used to set up AIN1 and AIN2 as either single-ended inputs or as a differential-ended input. Figure 10 shows an equivalent circuit of the differential input amplifier.

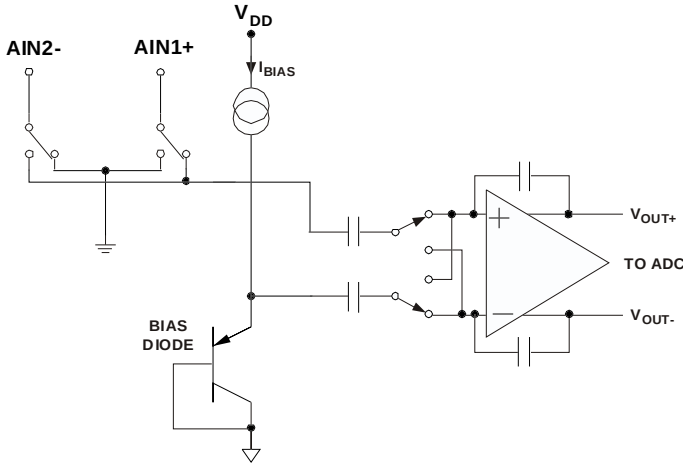


Figure 10. Differential-Ended Input Circuit

ADC DIFFERENTIAL-ENDED TRANSFER FUNCTION

The output coding of the ADT7411 differential-ended analog input is twos complement. The designed code transitions occur midway between successive integer LSB values (i.e. 1/2LSB, 3/2LSB, etc.). The LSB is 65mv/1024. The ideal transfer characteristic is shown in figure 12 below.

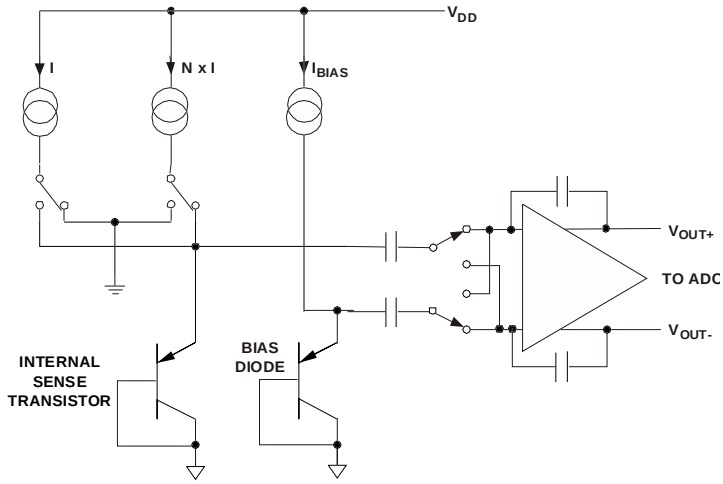


Figure 11. Top Level Structure of Internal Temperature Sensor

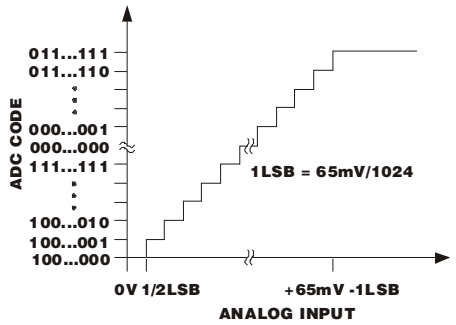


Figure 12. Differential-Ended Transfer Function

Use the following formula to translate the digital output value back into the differential-ended value. When DB9 is set to a 1 then the differential-ended value is negative.

Positive differential-ended input value : -

Differential-Ended Input Value = ADC Code*(d) x 1 LSB

*DB9 = 0

Negative differential-ended input value : -

Differential-Ended Input Value = (ADC Code*(d) - 1024) x 1 LSB

*DB9 = 1

The differential-ended data format is shown in Table 2.

TABLE 2. Differential-Ended Data Format

Differential-Ended Input Value	Digital Output
-32.5 mV	10 0000 0001
-30 mV	10 0010 1000
-25 mV	10 0111 0111
-20 mV	10 1100 0101
-15 mV	11 0001 0100
-10 mV	11 0110 0011
-5 mV	11 1011 0001
-63.48 µV	11 1111 1111
0	00 0000 0000
+63.48 µV	00 0000 0001
+5 mV	00 0100 1111
+10 mV	00 1001 1101
+15 mV	00 1110 1100
+20 mV	01 0011 1011
+25 mV	01 1000 1001
+30 mV	01 1101 1000
+32.5	01 1111 1111

AIN INTERRUPTS

The measured results from the AIN inputs are compared with the AIN V_{HIGH} and V_{LOW} limits. These voltage limits are stored in on-chip registers. Please note that the limit registers are 8 bits long while the AIN conversion result is 10 bits long. If the voltage limits are not masked out then any out of limit comparisons generate flags that are stored in Interrupt Status 1 Register (address = 00h) and one or more out-of limit results will cause the INTERRUPT output to pull either high or low depending on the output polarity setting.

Figure 13 showes the interrupt structure for the ADT7411. It gives a block diagram representation of how the various measurement channels affect the INTERRUPT pin.

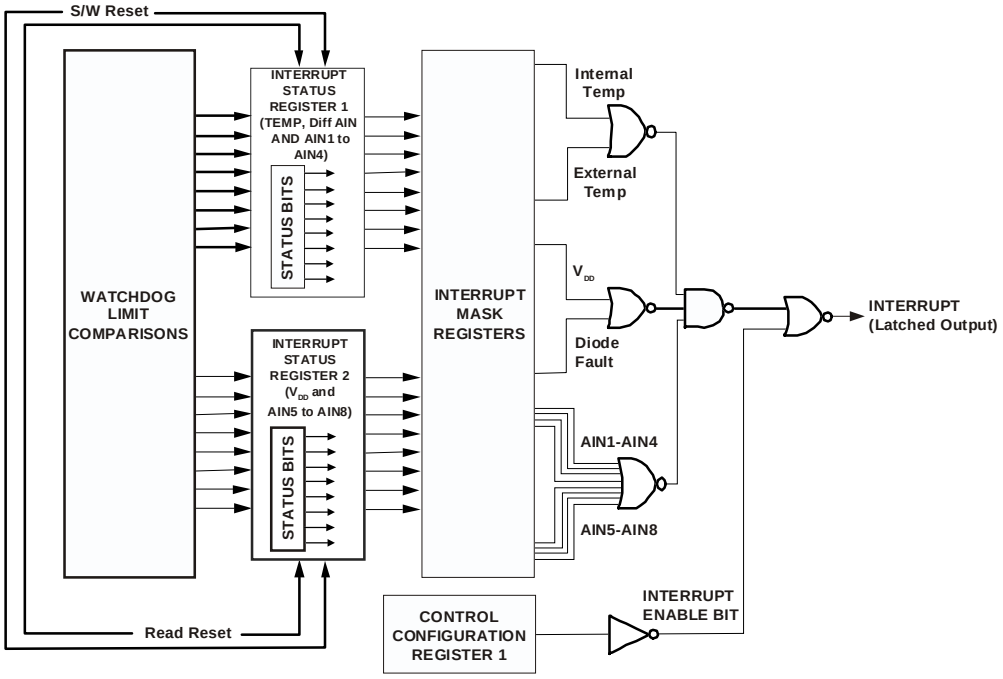


Figure 13. ADT7411 Interrupt Structure

FUNCTIONAL DESCRIPTION - TEMPERATURE AND V_{DD} MONITORING

POWER-UP TIME

On power-up it is important that no communication is initiated until 200ms after Vcc has settled. During this 200ms the part is performing a calibration routine and any communication to the device will interrupt this routine and could cause erroneous temperature measurements. V_{DD} must have settled to within 10% of it's final value after 50ms power-on time has elasped. Therefore once power is applied to the ADT7411, it can be addressed 250ms later. If it not possible to have V_{DD} at it's nominal value by the time 50ms has elasped then it is recommended that a measurement be taken on the V_{DD} channel before a temperature measurement is taken.

TEMPERATURE SENSOR

The ADT7411 contains an A to D converter with special input signal conditioning to enable operation with external and on-chip diode temperature sensors. When the ADT7411 is operating normally, the A to D converter operates in a free-running mode. When in Round Robin mode the analog input multiplexer sequently selects the V_{DD} input channel, on-chip temperature sensor to measure its internal temperature, the external temperature sensor or an AIN channel and then the rest of the AIN channels. These signals are digitized by the ADC and the results stored in the various Value Registers.

The measured results from the temperature sensors are compared with the Internal and External, T_{HIGH}, T_{LOW} limits. These temperature limits are stored in on-chip registers. If the temperature limits are not masked out then any out of limit comparisons generate flags that are stored in Interrupt Status 1 Register and one or more out-of limit results will cause the INTERRUPT output to pull either high or low depending on the output polarity setting.

Theoretically, the temperature sensor and ADC can measure temperatures from -128°C to +127°C with a resolution of 0.25°C. However, temperatures outside T_A are outside the guaranteed operating temperature range of the device. Temperature measurement from -128°C to +127°C is possible using an external sensor.

Temperature measurement is initiated by three methods. The first method is applicable when the part is in single channel measurement mode. It uses an internal clock countdown of 20ms and then a conversion is preformed. The internal oscillator is the only circuit that's powered up between conversions and once it times out, every 20ms, a wake-up signal is sent to power-up the rest of the circuitry. A monostable is activated at the beginning of the wake-up signal to ensure that sufficient time is given to the power-up process. The monostable typically takes 4 µs to time out. It then takes typically 25µs for each conversion to be completed. The temperature is measured 16 times and internally averaged to reduce noise. The total time to measure a temperature channel is typically 400us (25us x 16). The new temperature value is loaded into the Temperature Value Register and ready for reading by the I^2C or SPI interface. The user has the option of disabling the averaging by setting a bit (Bit 5) in the Control Configuration Register 2 (address 19h). The ADT7411 defaults on power-up with the averaging enabled.

Temperature measurement is also initiated after every read or write to the part when the part is in single channel measurement mode. Once serial communication has started, any conversion in progress is stopped and the ADC reset. Conversion will start again immediately after the serial communication has finished. The temperature measurement proceeds normally as described above. The same holds true for the AIN inputs.

The third method is applicable when the part is in round robin measurement mode. The part measures both the internal and external temperature sensors as it cycles through all possible measurement channels. The two temperature channels are measured each time the part runs a round robin sequence. In round robin mode the part is continously measuring.

V_{DD} MONITORING

The ADT7411 also has the capability of monitoring it's own power supply. The part measures the voltage on it's V_{DD} pin to a resolution of 10 bits. The resultant value is stored in two 8-bit registers, the two LSBs stored in register address 03h and the eight MSBs are stored in register address 06h. This allows the user to have the option of just doing a one byte read if 10-bit resolution is not important. The measured result is compared with V_{HIGH} and V_{LOW} limits. If the V_{DD} interrupt is not masked out then any out-of-limit comparison generates a flag in Interrupt Status 2 Register and one or more out-of-limit results will cause the INTERRUPT output to pull either high or low depending on the output polarity setting.

Measuring the voltage on the V_{DD} pin is regarded as monitoring a channel along with the Internal, External and AIN channels. You can select the V_{DD} channel for single channel measurement by setting Bit C4 = 1 and setting Bit 0 to Bit 2 to all 0's in Control Configuration 2 register.

When measuring the V_{DD} value the reference for the ADC is sourced from the Internal Reference. Table 3 shows the data format. As the max V_{CC} voltage measurable is 7 V, internal scaling is performed on the V_{CC} voltage to match the 2.25V internal reference value. Below is an example of how the transfer function works.

V_{DD} = 5 V

ADC Reference = 2.25 V

1 LSB = ADC Reference / 2^10 = 2.25 / 1024 = 2.197mV

Scale Factor = Fullscale V_{CC} / ADC Reference = 7 / 2.25 = 3.11

Conversion Result = V_{DD} / ((7/Scale Factor) x LSB size)

= 5 / (3.11 x 2.197mV)

= 2DBh

TABLE 3. V_{DD} Data Format, V_{REF} = 2.25 V

V_{DD} Value	Digital Output	
	Binary	Hex
2.5 V	01 0110 1110	16E
2.7 V	01 1000 1011	18B
3 V	01 1011 0111	1B7
3.5 V	10 0000 0000	200
4 V	10 0100 1001	249
4.5 V	10 1001 0010	292
5 V	10 1101 1011	2DB
5.5 V	11 0010 0100	324
6 V	11 0110 1101	36D
6.5 V	11 1011 0110	3B6
7 V	11 1111 1111	3FF

ON-CHIP REFERENCE

The ADT7411 has an on-chip 1.2 V band-gap refernece which is gained up by a switched capacitor amplifier to give an output of 2.25 V. The amplifier is only powered up at the start of the conversion phase and is powered down at the end of conversion. On power-up the default mode is to have the internal reference selected as the reference for the ADC. The internal reference is always used when measuring the internal and external temperature sensors.

ROUND ROBIN MEASUREMENT

On power-up the ADT7411 goes into Round Robin mode but monitoring is disabled. Setting Bit C0 of Configuration Register 1 to a 1 enables conversions. It sequences through all the available channels taking a measurement from each in the following order of V_{DD} , Internal temperature sensor, External temperature sensor/Differential Input/AIN1, AIN2, AIN3, AIN4, AIN5, AIN6, AIN7 and AIN8. Pin 7 and pin 8 can be configured to be either external temperature sensor pins, differential input pins or or stand alone analog input pins. At intervals of TBD ms another measurement cycle is performed on all channels. This method of taking a measurement on all the channels in one cycle is called Round Robin. Setting Bit 4 of Control Configuration 2 (address 19h) disables the Round Robin mode and in turn sets up the single channel mode. The single channel mode is where only one channel, eg. Internal temperature sensor, is measured in each conversion cycle.

The time taken to monitor all channels will normally not be of interest, as the most recently measured value can be read at any time.

For applications where the Round Robin time is important, it can be easily calculated.

As mentioned previously a conversion on each temperature channel takes TBD us and on the V_{DD}/AIN channels it takes TBD us. Each channel is measured 16 times and internally averaged to reduce noise.

A typical cycle time for eight AIN single-ended channels, V_{DD} channel and the Internal Temperature channel is therefore :

(16 x TBD) + (9 x 16 x TBD) = TBD ms

SINGLE CHANNEL MEASUREMENT

Setting C4 of Control Configuration 2 register enables the single channel mode and allows the ADT7411 to focus on one channel only. A channel is selected by writing to Bits 0:3 in register Control Configuration 2 register. For example, to select the V_{DD} channel for monitoring write to the Control Configuration 2 register and set C4 to 1 (if not done so already), then write all 0's to bits 0 to 3 . All subsequent conversions will be done on the V_{DD} channel only. To change the channel selection to the Internal temperature channel, write to the Control Configuration 2 register and set C0 = 1. When measuring in single channel mode there is a time delay of TBD us between each measurement. A measurement is also initiated after every read or write operation.

MEASUREMENT METHOD

INTERNAL TEMPERATURE MEASUREMENT

The ADT7411 contains an on-chip bandgap temperature sensor, whose output is digitized by the on-chip ADC. The temperature data is stored in the Internal Temperature Value Register. As both positive and negative temperatures can be measured, the temperature data is stored in two's complement format, as shown in Table 4. The thermal characteristics of the measurement sensor could change and therefore an offset is added to the measured value to enable the transfer function to match the thermal characteristics. This offset is added before the temperature data is stored. The offset value used is stored in the Internal Temperature Offset Register.

EXTERNAL TEMPERATURE MEASUREMENT

The ADT7411 can measure the temperature of one external diode sensor or diode-connected transistor.

The forward voltage of a diode or diode-connected transistor, operated at a constant current, exhibits a negative temperature coefficient of about -2mV/°C. Unfortunately, the absolute value of V_{be}, varies from device to device, and individual calibration is required to null this out, so the technique is unsuitable for mass-production.

The time taken to measure the external temperature can be reduced by setting C0 of Control Config. 3 register (1Ah). This increases the ADC clock speed from 1.4KHz to 22KHz but the analog filters on the D+ and D- input pins are switched off to accommodate the higher clock speeds. Running at the slower ADC speed, the time taken to measure the external temperature is TBD while on the fast ADC this time is reduced to TBD.

The technique used in the ADT7411 is to measure the change in V_{be} when the device is operated at two different currents.

This is given by:

$\Delta V_{be} = KT/q \times \ln(N)$

where:

K is Boltzmann's constant

q is charge on the carrier

T is absolute temperature in Kelvins

N is ratio of the two currents

Figure 7 shows the input signal conditioning used to measure the output of an external temperature sensor. This figure shows the external sensor as a substrate transistor, provided for temperature monitoring on some microprocessors, but it could equally well be a discrete transistor.

If a discrete transistor is used, the collector will not be grounded, and should be linked to the base. If a PNP transistor is used the base is connected to the D- input and the emitter to the D+ input. If an NPN transistor is used, the emitter is connected to the D- input and the base to the D+ input.

We recommend that a 2N3906 be used as the external transistor.

To prevent ground noise interfering with the measurement, the more negative terminal of the sensor is not referenced to ground, but is biased above ground by an internal diode at the D- input. As the sensor is operating in a noisy environment, C1 is provided as a noise filter. See the section on layout considerations for more information on C1.

To measure ΔV_{be}, the sensor is switched between operating currents of I and N x I. The resulting waveform is passed through a lowpass filter to remove noise, thence to a chopper-stabilized amplifier that performs the functions of amplification and rectification of the waveform to produce a DC voltage proportional to ΔV_{be}. This voltage is measured by the ADC to give a temperature output in 10-bit two's complement format. To further reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles.

LAYOUT CONSIDERATIONS

Digital boards can be electrically noisy environments, and care must be taken to protect the analog inputs from noise, particularly when measuring the very small voltages from a remote diode sensor. The following precautions should be taken:

1. Place the ADT7411 as close as possible to the remote sensing diode. Provided that the worst noise sources such as clock generators, data/address buses and CRTs are avoided, this distance can be 4 to 8 inches.
2. Route the D+ and D- tracks close together, in parallel, with grounded guard tracks on each side. Provide a ground plane under the tracks if possible.
3. Use wide tracks to minimize inductance and reduce noise pickup. 10 mil track minimum width and spacing is recommended.

Figure 14. Arrangement of Signal Tracks

4. Try to minimize the number of copper/solder joints, which can cause thermocouple effects. Where copper/solder joints are used, make sure that they are in both the D+ and D- path and at the same temperature.

   Thermocouple effects should not be a major problem as 1°C corresponds to about 240µV, and thermocouple voltages are about 3µV/°C of temperature difference. Unless there are two thermocouples with a big temperature differential between them, thermocouple voltages should be much less than 200mV.

5. Place 0.1µF bypass and 2200pF input filter capacitors close to the ADT7411.
6. If the distance to the remote sensor is more than 8 inches, the use of twisted pair cable is recommended. This will work up to about 6 to 12 feet.
7. For really long distances (up to 100 feet) use shielded twisted pair such as Belden #8451 microphone cable. Connect the twisted pair to D+ and D- and the shield to GND close to the ADT7411. Leave the remote end of the shield unconnected to avoid ground loops.

Because the measurement technique uses switched current sources, excessive cable and/or filter capacitance can affect the measurement. When using long cables, the filter capacitor may be reduced or removed.

Cable resistance can also introduce errors. 1Ω series resistance introduces about 0.5°C error.

TEMPERATURE VALUE FORMAT

One LSB of the ADC corresponds to 0.25°C. The ADC can theoretically measure a temperature span of 255 °C. The internal temperature sensor is guaranteed to a low value limit of -40 °C. It is possible to measure the full temperature span using the external temperature sensor. The temperature data format is shown in Table 4.

The result of the internal or external temperature measurements is stored as 2's complement format in the temperature value registers, and is compared with limits programmed into the Internal or External High and Low Registers.

TABLE 4. Temperature Data Format (Internal and External Temperature)

Temperature	Digital Output
-40 °C	11 0110 0000
-25 °C	11 1001 1100
-10 °C	11 1101 1000
-0.25 °C	11 1111 1111
0 °C	00 0000 0000
+0.25 °C	00 0000 0001
+10 °C	00 0010 1000
+25 °C	00 0110 0100
+50 °C	00 1100 1000
+75 °C	01 0010 1100
+100 °C	01 1001 0000
+105 °C	01 1010 0100
+125 °C	01 1111 0100

Temperature Conversion Formula:

1. Positive Temperature = ADC Code/4
2. Negative Temperature = (ADC Code* - 512)/4

*DB9 is removed from the ADC Code

ADT7411 REGISTERS

The ADT7411 contains registers that are used to store the results of external and internal temperature measurements, V_{DD} value measurements, analog input measurements, high and low temperature limits, supply voltage and analog input limits, configure multipurpose pins and generally control the device. A detailed description of these registers is given below.

The register map is divided into registers of 8-bits long. Each register has it's own indvidual address but some consist of data that is linked with other registers. These registers hold the 10-bit conversion results of measurements taken on the Temperature, V_{DD} and AIN channels. For example, the 8 MSBs of the V_{DD} measurement are stored in register address 06h while the 2 LSBs are stored in register address 03h. The link involved between these types of registers is that when the LSB register is read first then the MSB registers associated with that LSB register are locked to prevent any updates. To unlock these MSB registers the user has only to read to any one of them which will have the affect of unlocking all previously locked MSB registers. So for the example given above if register 03h was read first then MSB registers 06h and 07h would be locked to prevent any updates to them. If register 06h was read then this register and register 07h would be subsequently unlocked.

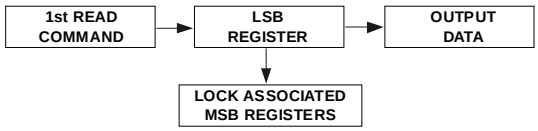


Figure 15. Phase 1 of 10-Bit Read

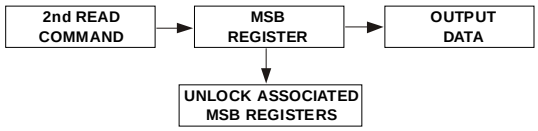


Figure 16. Phase 2 of 10-Bit Read

If an MSB register is read first, it's corresponding LSB register is not locked thus leaving the user with the option of just reading back 8 bits (MSB) of a 10-bit conversion result. Reading an MSB register first does not lock up other MSB registers and likewise reading an LSB register first does not lock up other LSB registers.

Table 5. List of ADT7411 Registers

RD/WR Address	Name	Power-on Default
00h	Interrupt Status 1	00h
01h	Interrupt Status 2	00h
02h	RESERVED	
03h	Internal Temp & V_{DD} LSBs	00h
04h	External Temp & AIN 1-4 LSBs	00h
05h	AIN 5 - 8 LSBs	00h
06h	V_{DD} MSBs	00h
07h	Internal Temperature MSBs	00h
08h	External Temp MSBs/Diff AIN/ AIN 1 MSBs	00h
09h	AIN 2 MSBs	00h
0Ah	AIN 3 MSBs	00h
0Bh	AIN 4 MSBs	00h
0Ch	AIN 5 MSBs	00h
0Dh	AIN 6 MSBs	00h
0Eh	AIN 7 MSBs	00h
0Fh	AIN 8 MSBs	00h
10h-17h	RESERVED	
18h	Control CONFIG 1	08h
19h	Control CONFIG 2	00h
1Ah	Control CONFIG 3	00h
1Bh-1Ch	RESERVED	
1Dh	Interrupt Mask 1	00h
1Eh	Interrput Mask 2	00h
1Fh	Internal Temp Offset	00h
20h	External Temp Offset	00h
21h	RESERVED	
22h	RESERVED	
23h	V_{DD} V_{HIGH} Limit	C9h
24h	V_{DD} V_{LOW} Limit	62h
25h	Internal T_{HIGH} Limit	64h
26h	Internal T_{LOW} Limit	C9h
27h	External T_{HIGH} / Diff AIN V_{HIGH} / AIN1 V_{HIGH} Limits	FFh
28h	External T_{LOW} / Diff AIN V_{LOW} / AIN1 V_{LOW} Limits	00h
29h-2Ah	RESERVED	
2Bh	AIN 2 V_{HIGH} Limit	FFh
2Ch	AIN 2 V_{LOW} Limit	00h
2Dh	AIN 3 V_{HIGH} Limit	FFh
2Eh	AIN 3 V_{LOW} Limit	00h
2Fh	AIN 4 V_{HIGH} Limit	FFh
30h	AIN 4 V_{LOW} Limit	00h
31h	AIN 5 V_{HIGH} Limit	FFh
32h	AIN 5 V_{LOW} Limit	00h
33h	AIN 6 V_{HIGH} Limit	FFh
34h	AIN 6 V_{LOW} Limit	00h
35h	AIN 7 V_{HIGH} Limit	FFh
36h	AIN 7 V_{LOW} Limit	00h
37h	AIN 8 V_{HIGH} Limit	FFh
38h	AIN 8 V_{LOW} Limit	00h
39h-4Ch	RESERVED	
4Dh	Device ID	02h
4Eh	Manufacturer's ID	41h
4Fh	Silicon Revision	00h
50h-FFh	RESERVED	

Interrupt Status 1 Register (Read only) [Add. = 00h]
This 8-bit read only register reflects the status of some of the interrupts that can cause the INTERRUPT pin to go active. This register is reset by a read operation or by a software reset.

Table 6. Interrupt Status 1 Register

D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

Bit	Function
D0	1 when Internal Temp Value exceeds T_{HIGH} limit
D1	1 when Internal Temp Value exceeds T_{LOW} limit
D2	This status bit is linked to the configuration of pins 7 and 8. If configured for External Temperature Sensor then this bit is 1 when External Temp Value exceeds T_{HIGH} limit. If configured for Differential Inputs then this bit is 1 when Differential Input Voltage exceeds V_{HIGH} or V_{LOW} limits. If configured for AIN1 and AIN2 then this bit is 1

	when AIN1 Input Voltage exceeds V_{HIGH} or V_{LOW} limits.
D3	1 when External Temp Value exceeds T_{LOW} limit
D4	1 indicates a fault (open or short) for the external temperature sensor.
D5	1 when AIN2 voltage exceeds V_{HIGH} or V_{LOW} limits.
D6	1 when AIN3 voltage exceeds V_{HIGH} or V_{LOW} limits.
D7	1 when AIN4 voltage exceeds V_{HIGH} or V_{LOW} limits.

Interrupt Status 2 Register (Read only) [Add. = 01h]
This 8-bit read only register reflects the status of the V_{DD} and AIN5-AIN8 interrupts that can cause the INTERRUPT pin to go active. This register is reset by a read operation or by a software reset.

Table 7. Interrupt Status 2 Register

D7	D6	D5	D4	D3	D2	D1	D0
N/A	N/A	N/A	0*	N/A	N/A	N/A	N/A

*Default settings at Power-up.

Bit	Function
D0	1 when AIN5 voltage exceeds V_{HIGH} or V_{LOW} limits.
D1	1 when AIN6 voltage exceeds V_{HIGH} or V_{LOW} limits.
D2	1 when AIN7 voltage exceeds V_{HIGH} or V_{LOW} limits.
D3	1 when AIN8 voltage exceeds V_{HIGH} or V_{LOW} limits.
D4	1 when V_{DD} value exceeds corrosponding V_{HIGH} and V_{LOW} limits
D5:D7	RESERVED

INTERNAL TEMPERATURE VALUE/V_{DD} VALUE REGISTER LSBs (Read only) [Add. = 03h]
This Internal Temperature Value and V_{DD} Value Register is a 8-bit read-only register. It stores the two LSBs of the 10-bit temperature reading from the internal temperature sensor and also the two LSBs of the 10-bit supply voltage reading.

Table 8. Internal Temp/V_{DD} LSBs

D7	D6	D5	D4	D3	D2	D1	D0
N/A	N/A	N/A	N/A	V1	LSB	T1	LSB
N/A	N/A	N/A	N/A	0*	0*	0*	0*

*Default settings at Power-up.

Bit	Function
D0	LSB of Internal Temperature Value
D1	B1 of Internal Temperature Value
D2	LSB of V_{DD} Value
D3	B1 of V_{DD} Value

EXTERNAL TEMPERATURE VALUE and ANALOG INPUTS 1-4 REGISTER LSBS (Read only) [Add. = 04h]
This is a 8-bit read-only register. Bits D2 - D7 store the two LSBs of the analog inputs AIN2 - AIN4. Bits D0 and D1 are used to store the two LSBs of either the External Temperature Value or AIN1 single-ended input value or Differential input value. The type of input for D0 and D1 is selected by Bits 1:2 of Control Configuration 1.

Table 9. External Temperature & AIN 1-4 LSBs

D7	D6	D5	D4	D3	D2	D1	D0
A4	$A4_{LSB}$	A3	$A3_{LSB}$	A2	$A2_{LSB}$	T/D/A	$T/D/A_{LSB}$
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

Bit	Function
D0	LSB of External Temperature Value or Analog Differential Value or AIN 1 Value
D1	Bit 1 of External Temperature Value or Analog Differential Value or AIN 1 Value
D2	LSB of AIN 2 Value
D3	Bit 1 of AIN 2 Value
D4	LSB of AIN 3 Value
D5	Bit 1 of AIN 3 Value
D6	LSB of AIN 4 Value
D7	Bit 1 of AIN 4 Value

ANALOG INPUTS 5-8 REGISTER LSBS (Read only) [Add. = 05h]
This is a 8-bit read-only register. Bits D0 - D7 store the two LSBs of the analog inputs AIN5 - AIN8. The MSBs are stored in registers 0Ch to 0Fh.

Table 10. External Temperature & AIN 1-4 LSBs

D7	D6	D5	D4	D3	D2	D1	D0
A8	$A8_{LSB}$	A7	$A7_{LSB}$	A6	$A6_{LSB}$	A5	$A5_{LSB}$
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

Bit	Function
D0	LSB of AIN 5 Value
D1	Bit 1 of AIN 5 Value
D2	LSB of AIN 6 Value
D3	Bit 1 of AIN 6 Value
D4	LSB of AIN 7 Value
D5	Bit 1 of AIN 7 Value
D6	LSB of AIN 8 Value
D7	Bit 1 of AIN 8 Value

V_{DD} VALUE REGISTER MSBS (Read only) [Add. = 06h]
This 8-bit read only register stores the supply voltage value. The 8 MSBs of the 10-bit value are stored in this register.

Table 11. V_{DD} Value MSBs

D7	D6	D5	D4	D3	D2	D1	D0
V9	V8	V7	V6	V5	V4	V3	V2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

INTERNAL TEMPERATURE VALUE REGISTER MSBS (Read only) [Add. = 07h]
This 8-bit read only register stores the Internal Temperature value from the internal temperature sensor in twos complement format. The 8 MSBs of the 10-bit value are stored in this register.

Table 12. Internal Temperature Value MSBs

D7	D6	D5	D4	D3	D2	D1	D0
T9	T8	T7	T6	T5	T4	T3	T2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

EXTERNAL TEMPERATURE VALUE OR DIFFERENTIAL INPUT VALUE OR ANALOG INPUT AIN 1 REGISTER MSBS (Read only) [Add. = 08h]
This 8-bit read only register stores, if selected, the External Temperature value or the Differential Input value or the Analog Input AIN 1 value. Selection is done in Control Configuration 1 register. The external temperature value and the differential input value are stored in twos complement format. The 8 MSBs of the 10-bit value are stored in this register.

Table 13. External Temperature Value/Analog Inputs MSBs

D7	D6	D5	D4	D3	D2	D1	D0
T/A9	T/A8	T/A7	T/A6	T/A5	T/A4	T/A3	T/A2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

AIN 2 REGISTER MSBS (Read) [Add. = 09h]
This 8-bit read register contains the 8 MSBs of the AIN 2 analog input voltage word. The value in this register is combined with bits D2:3 of the External Temperature Value and Analog Inputs 1-4 Register LSBs, address 04h, to give the full 10-bit conversion result of the analog value on the AIN 2 pin.

Table 14. AIN 2 MSBs

D7	D6	D5	D4	D3	D2	D1	D0
MSB	A8	A7	A6	A5	A4	A3	A2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

AIN 3 REGISTER MSBS (Read) [Add. = 0Ah]
This 8-bit read register contains the 8 MSBs of the AIN 3 analog input voltage word. The value in this register is combined with bits D4:5 of the External Temperature Value and Analog Inputs 1-4 Register LSBs, address 04h, to give the full 10-bit conversion result of the analog value on the AIN 3 pin.

Table 15. AIN 3 MSBs

D7	D6	D5	D4	D3	D2	D1	D0
MSB	A8	A7	A6	A5	A4	A3	A2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

AIN 4 REGISTER MSBS (Read) [Add. = 0Bh]
This 8-bit read register contains the 8 MSBs of the AIN 4 analog input voltage word. The value in this register is combined with bits D6:7 of the External Temperature Value and Analog Inputs 1-4 Register LSBs, address 04h, to give the full 10-bit conversion result of the analog value on the AIN 4 pin.

Table 16. AIN 4 MSBs

D7	D6	D5	D4	D3	D2	D1	D0
MSB	A8	A7	A6	A5	A4	A3	A2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

AIN 5 REGISTER MSBS (Read) [Add. = 0Ch]
This 8-bit read register contains the 8 MSBs of the AIN 5 analog input voltage word. The value in this register is combined with bits D0:1 of the Analog Inputs 5-8 Register LSBs, address 05h, to give the full 10-bit conversion result of the analog value on the AIN 5 pin.

Table 17. AIN 5 MSBs

D7	D6	D5	D4	D3	D2	D1	D0

MSB	A8	A7	A6	A5	A4	A3	A2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

AIN 6 REGISTER MSBS (Read) [Add. = 0Dh]
This 8-bit read register contains the 8 MSBs of the AIN 6 analog input voltage word. The value in this register is combined with bits D2:3 of the Analog Inputs 5-8 Register LSBs, address 05h, to give the full 10-bit conversion result of the analog value on the AIN 6 pin.

Table 18. AIN 6 MSBs

D7	D6	D5	D4	D3	D2	D1	D0
MSB	A8	A7	A6	A5	A4	A3	A2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

AIN 7 REGISTER MSBS (Read) [Add. = 0Eh]
This 8-bit read register contains the 8 MSBs of the AIN 7 analog input voltage word. The value in this register is combined with bits D4:5 of the Analog Inputs 5-8 Register LSBs, address 05h, to give the full 10-bit conversion result of the analog value on the AIN 7 pin.

Table 19. AIN 7 MSBs

D7	D6	D5	D4	D3	D2	D1	D0
MSB	A8	A7	A6	A5	A4	A3	A2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

AIN 8 REGISTER MSBS (Read) [Add. = 0Fh]
This 8-bit read register contains the 8 MSBs of the AIN 8 analog input voltage word. The value in this register is combined with bits D6:7 of the Analog Inputs 5-8 Register LSBs, address 05h, to give the full 10-bit conversion result of the analog value on the AIN 8 pin.

Table 20. AIN 8 MSBs

D7	D6	D5	D4	D3	D2	D1	D0
MSB	A8	A7	A6	A5	A4	A3	A2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

CONTROL CONFIGURATION 1 REGISTER (Read/ Write) [Add. = 18h]
This configuration register is an 8-bit read/write register that is used to setup some of the operating modes of the ADT7411.

Table 21. Control Configuration 1

D7	D6	D5	D4	D3	D2	D1	D0
PD	C6	C5	C4	C3	C2	C1	C0
0*	0*	0*	0*	1*	0*	0*	0*

*Default settings at Power-up.

Bit	Function
C0	This bit enables/disables conversions in Round Robin mode. ADT7411 powers up in Round Robin mode but monitoring is not initiated until this bit is set. Default = 0. 0 = Disable Round Robin monitoring. 1 = Enable Round Robin monitoring.
C2:C1	Selects between the three different analog inputs on pins 7 and 8. ADT7411 powers up with AIN1 and AIN2 selected. 00 AIN1 and AIN2 selected. 01 Differential AIN selected. 10 External TDM selected. 11 Undefined.
C3	RESERVED. Write 1 only to this bit.
C4	RESERVED. Write 0 only.
C5	0 Enable INTERRUPT 1 Disable INTERRUPT
C6	Configures INTERRUPT output polarity. 0 Active low 1 Active High
PD	Power-down Bit. Setting this bit to 1 puts the ADT7411 into standby mode. In this mode the analog circuitry is fully powered down, but serial interface is still operational. To power up the part again just write 0 to this bit.

CONTROL CONFIGURATION 2 REGISTER (Read/ Write) [Add. = 19h]
This configuration register is an 8-bit read/write register that is used to setup some of the operating modes of the ADT7411.

Table 22. Control Configuration 2

D7	D6	D5	D4	D3	D2	D1	D0
C7	C6	C5	C4	C3	C2	C1	C0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

Bit	Function
C3:0	In single channel mode these bits select between V_{DD}, the internal temperature sensor, external temperature sensor/Differential AIN/AIN1 and AIN2 to AIN8 for conversion. Default is V_{DD}. 0000 = V_{DD} 0001 = Internal Temperature Sensor. 0010 = External Temperature Sensor/Differential AIN/AIN1. 0011 = AIN2 0100 = AIN3 0101 = AIN4 0110 = AIN5 0111 = AIN6

	1000 = AIN7 1001 = AIN8 1010 - 1111 = RESERVED.
C4	Selects between single channel and Round Robin conversion cycle. Default is Round Robin. 0 = Round Robin. 1 = Single Channel.
C5	Default condition is to average every measurement on all channels 16 times. This bit disables this averaging. Channels comprise of temperature, analog inputs and V_{DD}. 0 = Enable averaging. 1 = Disable averaging.
C6	SMBus timeout on the serial clock puts a max limit on the pulse width of the clock. Ensures that a fault on the master SCL does not lock up the SDA line. 0 = Disable SMBus Timeout. 1 = Enable SMBus Timeout.
C7	Software Reset. Setting this bit to a 1 causes a software reset. All registers and DAC outputs will reset to their default settings.

CONTROL CONFIGURATION 3 REGISTER (Read/Write) [Add. = 1Ah]

This configuration register is an 8-bit read/write register that is used to setup some of the operating modes of the ADT7411.

Table 23. Control Configuration 3

D7	D6	D5	D4	D3	D2	D1	D0
C7	C6	C5	C4	C3	C2	C1	C0
0*	0*	0*	0*	1*	0*	0*	0*

*Default settings at Power-up.

Bit	Function
C0	Selects between fast and normal ADC conversion speeds. 0 = ADC clock at 1.4 KHz. 1 = ADC clock at 22.5 KHz. Analog filters are disabled.
C1:2	RESERVED. Only write 0's.
C3	RESERVED. Write only 1 to this bit.
C4	Selects the ADC reference to be either Internal V_{REF} or V_{DD} for analog inputs. 0 = Int V_{REF} 1 = V_{DD}
C5-C7	RESERVED. Only write 0's.

INTERRUPT MASK 1 REGISTER (Read/Write) [Add. = 1Dh]

This mask register is an 8-bit read/write register that can be used to mask out any interrupts that can can cause the INTERRUPT pin to go active.

Table 24. Interrupt Mask 1

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

Bit	Function
D0	0 = Enable internal T_{HIGH} interrupt. 1 = Disable internal T_{HIGH} interrupt.
D1	0 = Enable internal T_{LOW} interrupt. 1 = Disable internal T_{LOW} interrupt.
D2	0 = Enable external T_{HIGH} interrupt or Differential AIN interrupt or AIN1 interrupt. 1 = Disable external T_{HIGH} interrupt or Differential AIN interrupt or AIN1 interrupt.
D3	0 = Enable external T_{low} interrupt. 1 = Disable external T_{low} interrupt.
D4	0 = Enable external temperature fault interrupt. 1 = Disable external temperature fault interrupt.
D5	0 = Enable AIN2 interrupt. 1 = Disable AIN2 interrupt.
D6	0 = Enable AIN3 interrupt. 1 = Disable AIN3 interrupt.
D7	0 = Enable AIN4 interrupt. 1 = Disable AIN4 interrupt.

INTERRUPT MASK 2 REGISTER (Read/Write) [Add. = 1Eh]

This mask register is an 8-bit read/write register that can be used to mask out any interrupts that can can cause the INTERRUPT pin to go active.

Table 25. Interrupt Mask 2

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

Bit	Function
D0	0 = Enable AIN5 interrupt. 1 = Disable AIN5 interrupt.
D1	0 = Enable AIN6 interrupt. 1 = Disable AIN6 interrupt.
D2	0 = Enable AIN7 interrupt. 1 = Disable AIN7 interrupt.
D3	0 = Enable AIN8 interrupt. 1 = Disable AIN8 interrupt.
D4	0 = Enable V_{DD} interrupts. 1 = Disable V_{DD} interrupts.

D5:D7 RESERVED. Only write 0's.

INTERNAL TEMPERATURE OFFSET REGISTER (Read/Write) [Add. = 1Fh]
This register contains the Offset Value for the Internal Temperature Channel. A 2's complement number can be written to this register which is then 'added' to the measured result before it is stored or compared to limits. In this way a sort of one-point calibration can be done whereby the whole transfer function of the channel can be moved up or down. From a software point of view this may be a very simple method to vary the characteristics of the measurement channel if the thermal characteristics change. As it is an 8-bit register the temperature resolution is 1°C.

Table 26. Internal Temperature Offset

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

EXTERNAL TEMPERATURE OFFSET REGISTER (Read/Write) [Add. = 20h]
This register contains the Offset Value for the Internal Temperature Channel. A 2's complement number can be written to this register which is then 'added' to the measured result before it is stored or compared to limits. In this way a sort of one-point calibration can be done whereby the whole transfer function of the channel can be moved up or down. From a software point of view this may be a very simple method to vary the characteristics of the measurement channel if the thermal characteristics change. As it is an 8-bit register the temperature resolution is 1°C.

Table 27. External Temperature Offset

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

V_{DD} V_{HIGH} LIMIT REGISTER (Read/Write) [Add. = 23h]
This limit register is an 8-bit read/write register which stores the V_{DD} upper limit that will cause an interrupt and activate the INTERRUPT output (if enabled). For this to happen the measured V_{DD} value has to be greater than the value in this register. Default value is 5.5 V.

Table 28. V_{DD} V_{HIGH} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1*	1*	0*	0*	1*	0*	0*	1*

*Default settings at Power-up.

V_{DD} V_{LOW} LIMIT REGISTER (Read/Write) [Add. = 24h]
This limit register is an 8-bit read/write register which stores the V_{DD} lower limit that will cause an interrupt and activate the INTERRUPT output (if enabled). For this to happen the measured V_{DD} value has to be less than the value in this register. Default value is 2.7 V.

Table 29. V_{DD} V_{HIGH} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	1*	1*	0*	0*	0*	1*	0*

*Default settings at Power-up.

INTERNAL T_{HIGH} LIMIT REGISTER (Read/Write) [Add. = 25h]
This limit register is an 8-bit read/write register which stores the 2's complement of the internal temperature upper limit that will cause an interrupt and activate the INTERRUPT output (if enabled). For this to happen the measured Internal Temperature Value has to be greater than the value in this register. As it is an 8-bit register the temperature resolution is 1°C. Default value is +40°C.

Table 30. Internal T_{HIGH} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	1*	0*	1*	0*	0*	0*

*Default settings at Power-up.

INTERNAL T_{LOW} LIMIT REGISTER (Read/Write) [Add. = 26h]
This limit register is an 8-bit read/write register which stores the 2's complement of the internal temperature lower limit that will cause an interrupt and activate the INTERRUPT output (if enabled). For this to happen the measured Internal Temperature Value has to be more negative than the value in this register. As it is an 8-bit register the temperature resolution is 1°C. Default value is -25°C.

Table 31. Internal T_{LOW} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1*	1*	1*	0*	0*	1*	1*	1*

*Default settings at Power-up.

EXTERNAL T_{HIGH} / DIFF AIN V_{HIGH} / AIN1 V_{HIGH} LIMIT REGISTER (Read/Write) [Add. = 27h]
If pins 7 and 8 are configured for the external temperature sensor then this limit register is an 8-bit read/write register which stores the 2's complement of the external temperature upper limit that will cause an interrupt and activate the INTERRUPT output (if enabled). For this to happen the measured External Temperature Value has to be greater than the value in this register. As it is an 8-bit register the temperature resolution is 1°C.

If pins 7 and 8 are configured for differential input then this limit register is an 8-bit read/write register which stores the 2's complement of the Differential AIN input upper limit that will cause an interrupt and activate the INTERRUPT output (if enabled). For this to happen the measured Differential AIN value has to be greater than the value in this register. As it is an 8-bit register the resolution is four times less than the resolution of the 10-Bit ADC.

If pins 7 and 8 are configured for AIN1 and AIN2 single-ended inputs then this limit register is an 8-bit read/write register which stores the AIN1 input upper limit that will cause an interrupt and activate the INTERRUPT output (if enabled). For this to happen the measured AIN1 value has to be greater than the value in this register. As it is an 8-bit register the resolution is four times less than the resolution of the 10-Bit ADC. As the power-up default settings for pins 7 and 8 is AIN1 and AIN2 single-ended inputs then the default value for this limit register is fullscale voltage.

Table 32. AIN1 V_{HIGH} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1*	1*	1*	1*	1*	1*	1*	1*

*Default settings at Power-up.

EXTERNAL T_{LOW} / DIFF AIN V_{LOW} / AIN1 V_{LOW} LIMIT REGISTER (Read/Write) [Add. = 28h]
If pins 7 and 8 are configured for the external temperature sensor then this limit register is an 8-bit read/write register which stores the 2's complement of the external temperature lower limit that will cause an interrupt and activate the INTERRUPT output (if enabled). For this to happen the measured External Temperature Value has to be more negative than the value in this register. As it is an 8-bit register the temperature resolution is 1°C.

If pins 7 and 8 are configured for differential input then this limit register is an 8-bit read/write register which stores the 2's complement of the Differential AIN input lower limit that will cause an interrupt and activate the INTERRUPT output (if enabled). For this to happen the measured Differential AIN value has to be less than the value in this register. As it is an 8-bit register the resolution is four times less than the resolution of the 10-Bit ADC.

If pins 7 and 8 are configured for AIN1 and AIN2 single-ended inputs then this limit register is an 8-bit read/write register which stores the AIN1 input lower limit that will cause an interrupt and activate the INTERRUPT output (if enabled). For this to happen the measured AIN1 value has to be less than the value in this register. As it is an 8-bit register the resolution is four times less than the resolution of the 10-Bit ADC. As the power-up default settings for pins 7 and 8 is AIN1 and AIN2 single-ended inputs then the default value for this limit register is 0 V.

Table 33. AIN1 V_{LOW} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

AIN2 V_{HIGH} LIMIT REGISTER (Read/Write) [Add. = 2Bh]
This limit register is an 8-bit read/write register which stores the AIN2 input upper limit that will cause an interrupt and activate the INTERRUPT output (if enabled). For this to happen the measured AIN2 value has to be greater than the value in this register. As it is an 8-bit register the resolution is four times less than the resolution of the 10-Bit ADC. Default value is fullscale voltage.

Table 34. AIN2 V_{HIGH} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1*	1*	1*	1*	1*	1*	1*	1*

*Default settings at Power-up.

AIN2 V_{LOW} LIMIT REGISTER (Read/Write) [Add. = 2Ch]
This limit register is an 8-bit read/write register which stores the AIN2 input lower limit that will cause an interrupt and activate the INTERRUPT output (if enabled). For this to happen the measured AIN2 value has to be less than the value in this register. As it is an 8-bit register the resolution is four times less than the resolution of the 10-Bit ADC. Default value is 0 V.

Table 35. AIN2 V_{LOW} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

AIN3 V_{HIGH} LIMIT REGISTER (Read/Write) [Add. = 2Dh]
This limit register is an 8-bit read/write register which stores the AIN3 input upper limit that will cause an interrupt and activate the INTERRUPT output (if enabled). For this to happen the measured AIN3 value has to be greater than the value in this register. As it is an 8-bit register the resolution is four times less than the resolution of the 10-Bit ADC. Default value is fullscale voltage.

Table 36. AIN3 V_{HIGH} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1*	1*	1*	1*	1*	1*	1*	1*

*Default settings at Power-up.

AIN3 V_{LOW} LIMIT REGISTER (Read/Write) [Add. = 2Eh]
This limit register is an 8-bit read/write register which stores the AIN3 input lower limit that will cause an interrupt and activate the INTERRUPT output (if enabled). For this to happen the measured AIN3 value has to be less than the value in this register. As it is an 8-bit register the resolution is four times less than the resolution of the 10-Bit ADC. Default value is 0 V.

Table 37. AIN3 V_{LOW} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

AIN4 V_{HIGH} LIMIT REGISTER (Read/Write) [Add. = 2Fh]
This limit register is an 8-bit read/write register which stores the AIN4 input upper limit that will cause an interrupt and activate the INTERRUPT output (if enabled). For this to happen the measured AIN4 value has to be greater than the value in this register. As it is an 8-bit register the resolution is four times less than the resolution of the 10-Bit ADC. Default value is fullscale voltage.

Table 38. AIN4 V_{HIGH} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1*	1*	1*	1*	1*	1*	1*	1*

*Default settings at Power-up.

AIN4 V_{LOW} LIMIT REGISTER (Read/Write) [Add. = 30h]
This limit register is an 8-bit read/write register which stores the AIN4 input lower limit that will cause an interrupt and activate the INTERRUPT output (if enabled). For this to happen the measured AIN4 value has to be less than the value in this register. As it is an 8-bit register the resolution is four times less than the resolution of the 10-Bit ADC. Default value is 0 V.

Table 39. AIN4 V_{LOW} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

AIN5 V_{HIGH} LIMIT REGISTER (Read/Write) [Add. = 31h]
This limit register is an 8-bit read/write register which stores the AIN5 input upper limit that will cause an interrupt and activate the INTERRUPT output (if enabled). For this to happen the measured AIN5 value has to be greater than the value in this register. As it is an 8-bit register the resolution is four times less than the resolution of the 10-Bit ADC. Default value is fullscale voltage.

Table 40. AIN5 V_{HIGH} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1*	1*	1*	1*	1*	1*	1*	1*

*Default settings at Power-up.

AIN5 V_{LOW} LIMIT REGISTER (Read/Write) [Add. = 32h]
This limit register is an 8-bit read/write register which stores the AIN5 input lower limit that will cause an interrupt and activate the INTERRUPT output (if enabled). For this to happen the measured AIN5 value has to be less than the value in this register. As it is an 8-bit register the resolution is four times less than the resolution of the 10-Bit ADC. Default value is 0 V.

Table 41. AIN5 V_{LOW} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

AIN6 V_{HIGH} LIMIT REGISTER (Read/Write) [Add. = 33h]
This limit register is an 8-bit read/write register which stores the AIN3 input upper limit that will cause an interrupt and activate the INTERRUPT output (if enabled). For this to happen the measured AIN6 value has to be greater than the value in this register. As it is an 8-bit register the resolution is four times less than the resolution of the 10-Bit ADC. Default value is fullscale voltage.

Table 42. AIN6 V_{HIGH} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

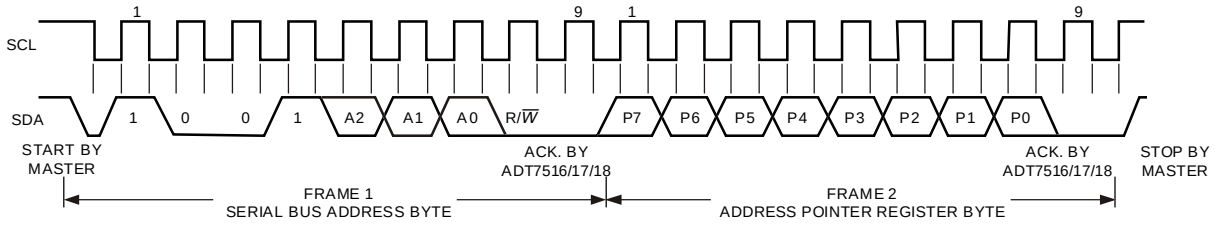


Figure 17. I^2C - Writing to the Address Pointer Register to select a register for a subsequent Read operation

1*	1*	1*	1*	1*	1*	1*	1*

*Default settings at Power-up.

AIN6 V_{LOW} LIMIT REGISTER (Read/Write) [Add. = 34h]
This limit register is an 8-bit read/write register which stores the AIN6 input lower limit that will cause an interrupt and activate the INTERRUPT output (if enabled). For this to happen the measured AIN6 value has to be less than the value in this register. As it is an 8-bit register the resolution is four times less than the resolution of the 10-Bit ADC. Default value is 0 V.

Table 43. AIN6 V_{LOW} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

AIN7 V_{HIGH} LIMIT REGISTER (Read/Write) [Add. = 35h]
This limit register is an 8-bit read/write register which stores the AIN7 input upper limit that will cause an interrupt and activate the INTERRUPT output (if enabled). For this to happen the measured AIN7 value has to be greater than the value in this register. As it is an 8-bit register the resolution is four times less than the resolution of the 10-Bit ADC. Default value is fullscale voltage.

Table 44. AIN7 V_{HIGH} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1*	1*	1*	1*	1*	1*	1*	1*

*Default settings at Power-up.

AIN7 V_{LOW} LIMIT REGISTER (Read/Write) [Add. = 36h]
This limit register is an 8-bit read/write register which stores the AIN7 input lower limit that will cause an interrupt and activate the INTERRUPT output (if enabled). For this to happen the measured AIN7 value has to be less than the value in this register. As it is an 8-bit register the resolution is four times less than the resolution of the 10-Bit ADC. Default value is 0 V.

Table 45. AIN7 V_{LOW} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

AIN8 V_{HIGH} LIMIT REGISTER (Read/Write) [Add. = 37h]
This limit register is an 8-bit read/write register which stores the AIN8 input upper limit that will cause an interrupt and activate the INTERRUPT output (if enabled). For this to happen the measured AIN8 value has to be greater than the value in this register. As it is an 8-bit register the resolution is four times less than the resolution of the 10-Bit ADC. Default value is fullscale voltage.

Table 46. AIN8 V_{HIGH} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1*	1*	1*	1*	1*	1*	1*	1*

*Default settings at Power-up.

AIN8 V_{LOW} LIMIT REGISTER (Read/Write) [Add. = 38h]
This limit register is an 8-bit read/write register which stores the AIN8 input lower limit that will cause an interrupt and activate the INTERRUPT output (if enabled). For this to happen the measured AIN8 value has to be less than the value in this register. As it is an 8-bit register the resolution is four times less than the resolution of the 10-Bit ADC. Default value is 0 V.

Table 47. AIN8 V_{LOW} Limit

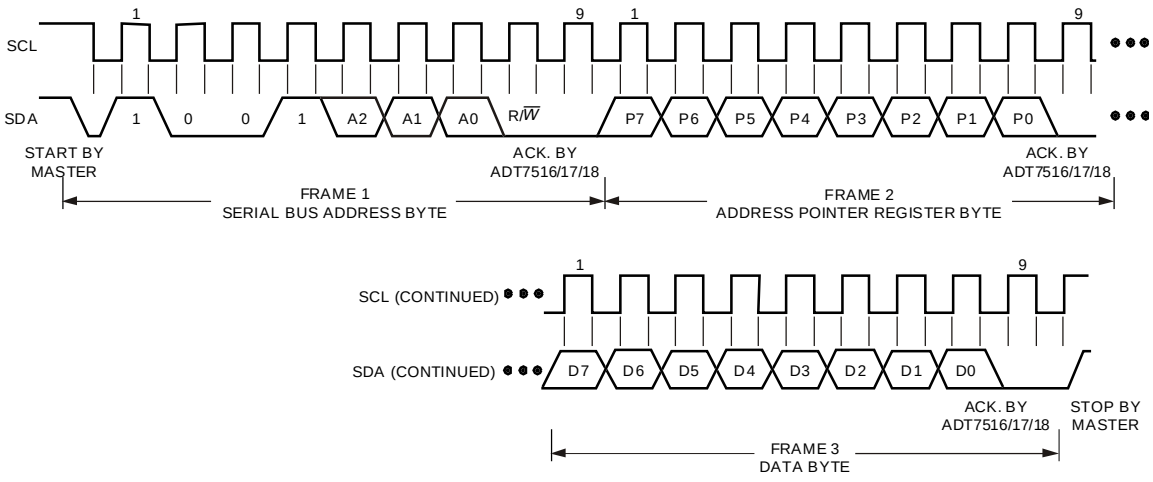


Figure 18. I^2C - Writing to the Address Pointer Register followed by a single byte of data to the selected register

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at Power-up.

DEVICE ID REGISTER (Read only) [Add. = 4Dh]
This 8-bit read only register gives an unique identification number for this part. ADT7411 = 02h.

MANUFACTURER'S ID REGISTER (Read only) [Add. = 4Eh]
This register contains the manufacturers identification number. ADI's is 41h.

SILICON REVISION REGISTER (Read only) [Add. = 4Fh]
This register is divided into the four lsbs representing the Stepping and the four msbs representing the Version. The Stepping contains the manufacturers code for minor revisions or steppings to the silicon. The Version is the ADT7411 version number. The ADT7411's version number is 0000b.

ADT7411 SERIAL INTERFACE
There are two serial interfaces that can be used on this part, I^2C and SPI. A valid serial communication protocol selects the type of interface.

SERIAL INTERFACE SELECTION
The $\overline{CS}$ line controls the selection between I^2C and SPI. If $\overline{CS}$ is held high during a valid I^2C communication then the serial interface selects the I^2C mode once the correct serial bus address has been recognised.
To set the interface to SPI mode the $\overline{CS}$ line must be low during a valid SPI communication. This will cause the interface to select the SPI mode once the correct read or write command has been recognised. As per most SPI standards the $\overline{CS}$ line must be low during every SPI communication to the ADT7411 and high all other times.

The following sections describe in detail how to use these interfaces.

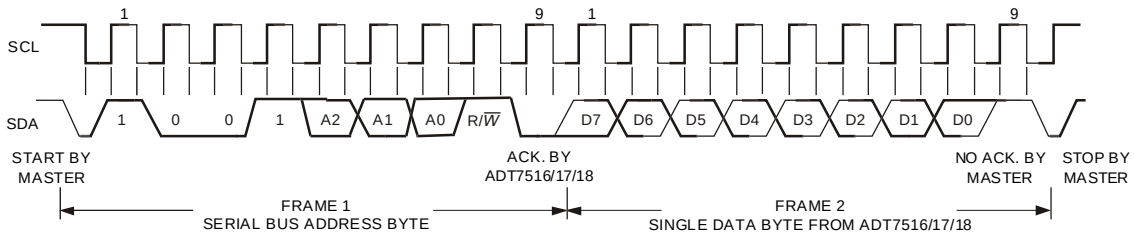


Figure 19. I^2C - Reading a single byte of data from a selected register

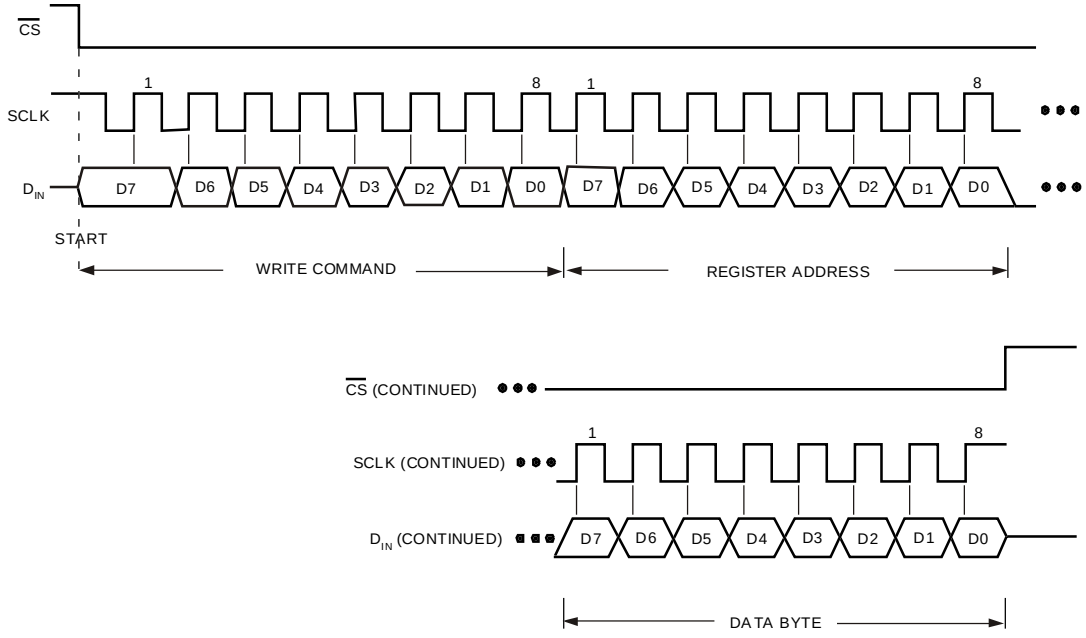


Figure 20. SPI - Writing to the Address Pointer Register followed by a single byte of data to the selected register

I²C SERIAL INTERFACE

Like all I²C-compatible devices, the ADT7411 has an 7-bit serial address. The four MSBs of this address for the ADT7411 are set to 1001. The three LSBs are set by pin 11, ADD. The ADD pin can be configured three ways to give three different address options; low, floating and high. Setting the ADD pin low gives a serial bus address of 1001 000, leaving it floating gives the address 1001 010 and setting it high gives the address 1001 011.

There is a programmable SMBus timout. When this is enabled the SMBus will timeout after 25 ms of no activity. To enable it, set Bit 6 of Control Configuration 2 register. The power-up default is with the SMBus timeout disabled.

The ADT7411 supports SMBus Packet Error Checking (PEC) and it's use is optional. It is triggered by supplying the extra clocks for the PEC byte. The PEC is calculated using CRC-8. The Frame Clock Sequence (FCS) conforms to CRC-8 by the polynominal :

$$C(x) = x^8 + x^2 + x^1 + 1$$

Consult SMBus specification for more information.

The serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, defined as a high to low transition on the serial data line SDA whilst the serial clock line SCL remains high. This indicates that an address/data stream will follow. All slave peripherals connected to the serial bus respond to the START condition, and shift in the next 8 bits, consisting of a 7-bit address (MSB first) plus a R/$\overline{W}$ bit, which determines the direction of the data transfer, i.e. whether data will be written to or read from the slave device.

   The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the Acknowledge Bit. All other devices on the bus now remain idle whilst the selected device waits for data to be read from or written to it. If the R/$\overline{W}$ bit is a 0 then the master will write to the slave device. If the R/$\overline{W}$ bit is a 1 the master will read from the slave device.
2. Data is sent over the serial bus in sequences of 9 clock pulses, 8 bits of data followed by an Acknowledge Bit from the receiver of data. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, as a low to high transition when the clock is high may be interpreted as a STOP signal.
3. When all data bytes have been read or written, stop conditions are established. In WRITE mode, the master will pull the data line high during the 10th clock pulse to assert a STOP condition. In READ mode, the master device will pull the data line high during the low

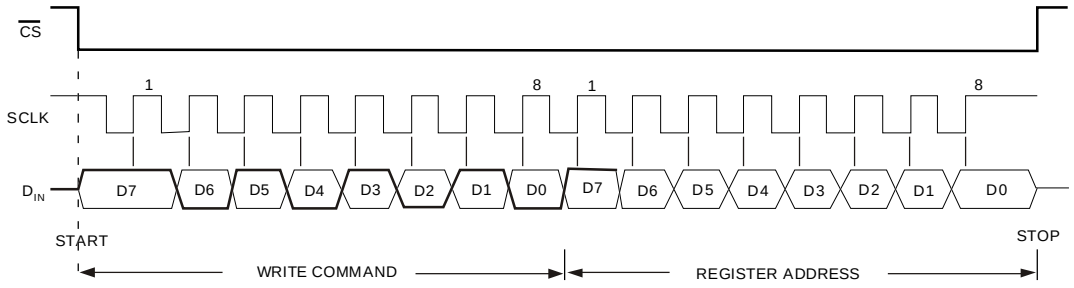


Figure 21. SPI - Writing to the Address Pointer Register to select a register for a subsequent read operation

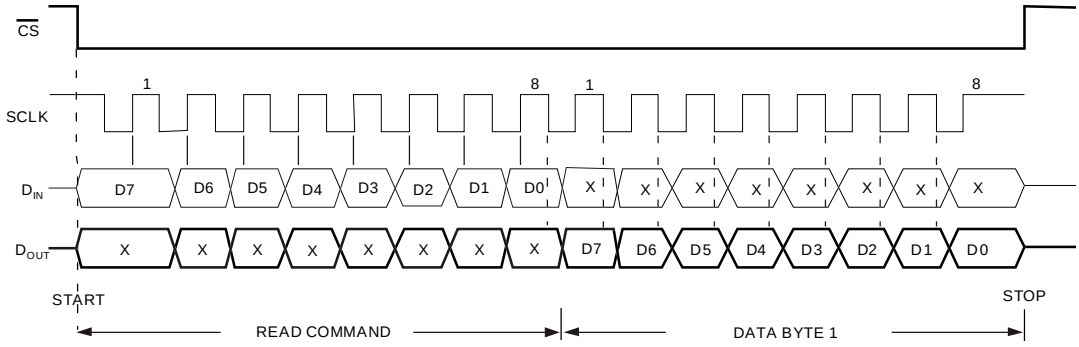


Figure 22. SPI - Reading a single byte of data from a selected register

period before the 9th clock pulse. This is known as No Acknowledge. The master will then take the data line low during the low period before the 10th clock pulse, then high during the 10th clock pulse to assert a STOP condition.

Any number of bytes of data may be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation, because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

WRITING TO THE ADT7411

Depending on the register being written to, there are two different writes for the ADT7411. It is not possible to do a block write to this part i.e no I^2C auto-increment.

Writing to the Address Pointer Register for a subsequent read.

In order to read data from a particular register, the Address Pointer Register must contain the address of that register. If it does not, the correct address must be written to the Address Pointer Register by performing a single-byte write operation, as shown in Figure 17. The write operation consists of the serial bus address followed by the address pointer byte. No data is written to any of the data registers. A read operation is then performed to read the register.

Writing data to a Register.

All registers are 8-bit registers so only one byte of data can be written to each register. Writing a single byte of data to one of these Read/Write registers consists of the serial bus address, the data register address written to the Address Pointer Register, followed by the data byte written to the selected data register. This is illustrated in Figure 18. To write to a different register, another START or repeated START is required. If more than one byte of data is sent in one communication operation, the addressed register will be repeately loaded until the last data byte has been sent.

READING DATA FROM THE ADT7411

Reading data from the ADT7411 is done in a one byte operation. Reading back the contents of a register is shown in Figure 19. The register address previously having been set up by a single byte write operation to the Address Pointer Register. If you want to read from another register then you will have to write to the Address Pointer Register again to set up the relevant register address. Thus block reads are not possible i.e. no I^2C auto-increment.

SPI SERIAL INTERFACE

The SPI serial interface of the ADT7411 consists of four wires, $\overline{CS}$, SCLK, DIN and DOUT. The $\overline{CS}$ is used to select the device when more than one device is connected to the serial clock and data lines. The SCLK is used to clock data in and out of the part. The DIN line is used to write to the registers and the DOUT line is used to read data back from the registers.

The part operates in a slave mode and requires an externally applied serial clock to the SCLK input. The serial interface is designed to allow the part to be interfaced to systems that provide a serial clock that is synchronized to the serial data.

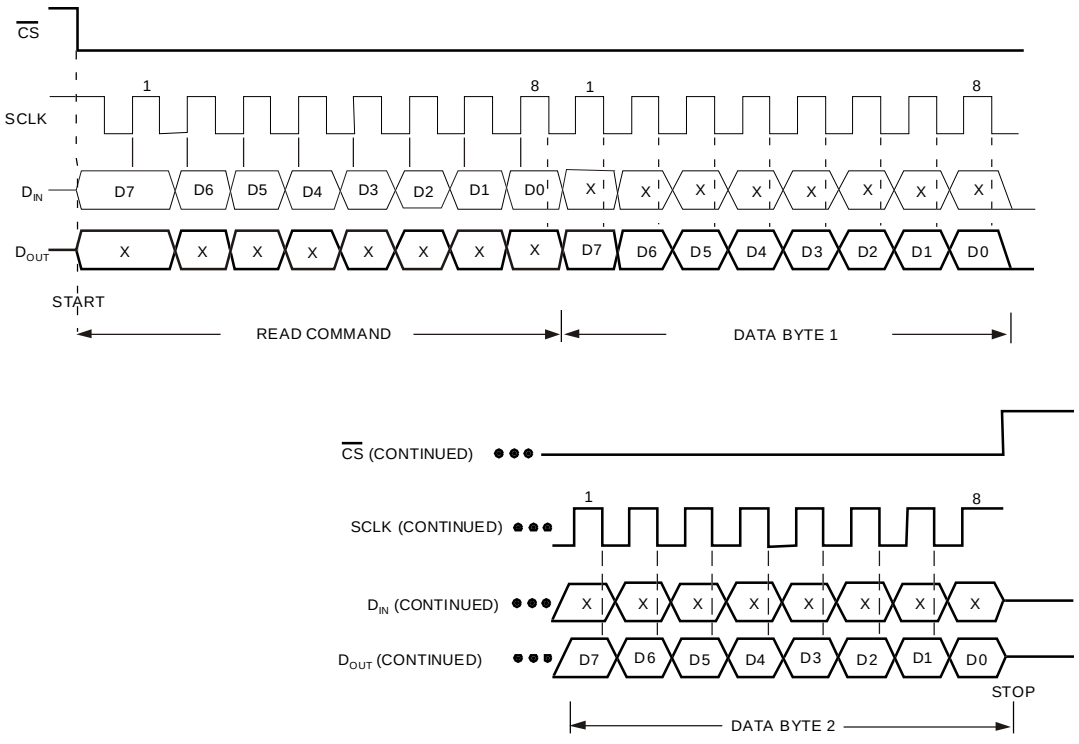


Figure 23. SPI - Reading a two bytes of data from two sequential registers

There are two types of serial operations, a read and a write. Command words are used to distinguish between a read and a write operation. These command words are given in Table 48. Address auto-increment is possible in SPI mode.

Table 48. SPI COMMAND WORDS

WRITE	READ
90h (1001 0000)	91h (1001 0001)

Write Operation

Figure 20 shows the timing diagram for a write operation to the ADT7411. Data is clocked into the registers on the rising edge of SCLK. When the $\overline{CS}$ line is high the DIN and DOUT lines are in three-state mode. Only when the $\overline{CS}$ goes from a high to a low does the part accept any data on the DIN line. In SPI mode the Address Pointer Register is capable of auto-incrementing to the next register in the register map without having to load the Address Pointer register each time. In Figure 20 the register address portion of the diagram gives the first register that will be written to. Subsequent data bytes will be written into sequential writable registers. Thus after each data byte has been written into a register, the Address Pointer Register auto increments it's value to the next available register. The Address Pointer Register will auto-increment from 00h to 3Fh and will loop back to start all over again at 00h when it reaches 3Fh.

Read Operation

Figures 21 to 23 show the timing diagrams necessary to accomplish correct read operations. To read back from a register you first have to write to the Address Pointer Register with the address of the register you wish to read from. This operation is shown in Figure 21. Figure 22 shows the procedure for reading back a single byte of data. The read command is first sent to the part during the first 8 clock cycles, during the following 8 clock cycles the data contained in the register selected by the Address Pointer register is outputted onto the DOUT line. Data is outputted onto the DOUT line on the falling edge of SCLK. Figure 23 shows the procedure when reading data from two sequential registers. Multiple data reads are possible in SPI interface mode as the Address Pointer Register is auto-incremental. The Address Pointer Register will auto-increment from 00h to 3Fh and will loop back to start all over again at 00h when it reaches 3Fh.

SMBUS/SPI INTERRUPT

The ADT7411 INTERRUPT output is an interrupt line for devices that want to trade their ability to master for an extra pin. The ADT7411 is a slave only device and uses the SMBus/SPI INTERRUPT to signal the host device that it wants to talk. The SMBus/SPI INTERRUPT on the ADT7411 is used as an over/under limit indicator.

The INTERRUPT pin has an open-drain configuration which allows the outputs of several devices to be wired-AND together when the INTERRUPT pin is active low. Use D6 of the Control Configuration 1 Register to set the active polarity of the INTERRUPT output. The power-up default is active low. The INTERRUPT function can be disabled or enabled by setting D5 of Control Configuration 1 Register to a 1 or 0 respectively.

The INTERRUPT output becomes active when either the Internal Temperature Value, the External Temperature Value, V_{DD} Value or any of the AIN input values exceed the values in their corresponding T_{HIGH}/V_{HIGH} or T_{LOW}/V_{LOW} Registers. The INTERRUPT output goes inactive again when a conversion result has the measured value back within the trip limits.

The INTERRUPT output requires an external pull-up resistor. This can be connected to a voltage different from V_{DD} provided the maximum voltage rating of the INTERRUPT output pin is not exceeded. The value of the pull-up resistor depends on the application, but should be as large enough to avoid excessive sink currents at the INTERRUPT output, which can heat the chip and affect the temperature reading.

Outline Dimensions
(Dimensions shown in inches and mm)
16-Lead QSOP Package
(RQ-16)