DATA SHEET

PCA9552

16-bit I^2C LED driver with programmable blink rates

Product data

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Philips
Semiconductors

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16-bit I²C LED driver with programmable blink rates

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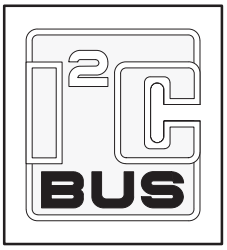


FEATURES

- 16 LED drivers (on, off, flashing at a programmable rate)
- 2 selectable, fully programmable blink rates (frequency and duty cycle) between 0.15625 and 40 Hz (6.4 and 0.025 seconds)
- Input/outputs not used as LED drivers can be used as regular GPIOs
- Internal oscillator requires no external components
- I²C interface logic compatible with SMBus
- Internal power-on reset
- Noise filter on SCL/SDA inputs
- Active low reset input
- 16 open drain outputs directly drive LEDs to 25 mA
- Edge rate control on outputs
- No glitch on power-up
- Supports hot insertion
- Low stand-by current
- Operating power supply voltage range of 2.3 V to 5.5 V
- 0 to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 150 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA
- Package offer: SO 24, TSSOP 24, HVQFN24

DESCRIPTION

The PCA9552 LED Blinker blinks LEDs in I²C and SMBus applications where it is necessary to limit bus traffic or free up the I²C Master's (MCU, MPU, DSP, chipset, etc.) timer. The uniqueness of this device is the internal oscillator with two programmable blink rates. To blink LEDs using normal I/O Expanders like the PCF8574 or PCA9554, the bus master must send repeated commands to turn the LED on and off. This greatly increases the amount of traffic on the I²C bus and uses up one of the master's timers. The PCA9552 LED Blinker instead requires only the initial set up command to program BLINK RATE 1 and BLINK RATE 2 (i.e., the frequency and duty cycle) for each individual output. From then on, only one command from the bus master is required to turn each individual open drain output ON, OFF, or to cycle at BLINK RATE 1 or BLINK RATE 2. Maximum output sink current is 25 mA per bit and 200 mA per package.

Any bits not used for controlling the LEDs can be used for General Purpose Parallel Input/Output (GPIO) expansion.

The active low hardware reset pin ($\overline{\text{RESET}}$) and Power On Reset (POR) initializes the registers to their default state, all zeroes, causing the bits to be set high (LED off).

Three hardware address pins on the PCA9552 allow eight devices to operate on the same bus.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DRAWING NUMBER
24-pin plastic SO	–40 to +85 °C	PCA9552D	PCA9552D	SOT137-1
24-pin plastic TSSOP	–40 to +85 °C	PCA9552PW	PCA9552PW	SOT355-1
24-pin plastic HVQFN	–40 to +85 °C	PCA9552BS	9552	SOT616-1

Standard packing quantities and other packaging data is available at www.philipslogic.com/packaging.

I²C is a trademark of Philips Semiconductors Corporation.

PIN CONFIGURATION — SO, TSSOP

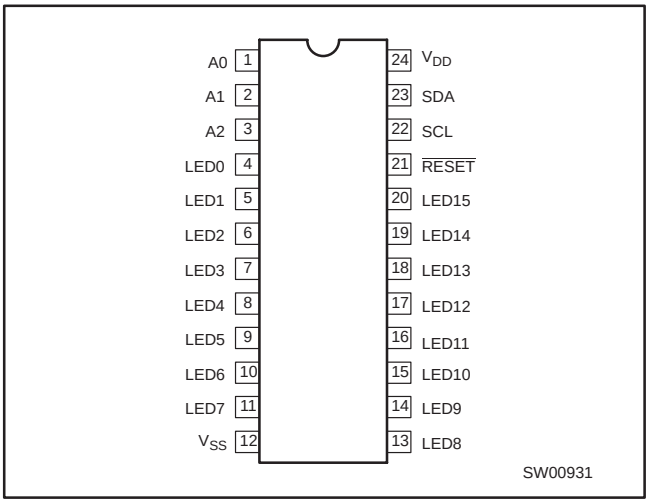


Figure 1. Pin configuration — SO, TSSOP

PIN CONFIGURATION — HVQFN

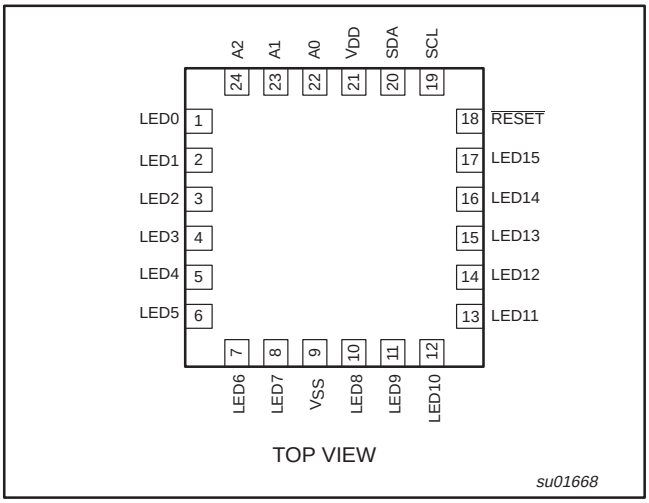


Figure 2. Pin configuration — HVQFN

PIN DESCRIPTION

SO, TSSOP PIN NUMBER	HVQFN PIN NUMBER	SYMBOL	FUNCTION
1	22	A0	Address input 0
2	23	A1	Address input 1
3	24	A2	Address input 2
4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8	LED0–7	LED driver 0–7
12	9	V_{SS}	Supply ground
13, 14, 15, 16, 17, 18, 19, 20	10, 11, 12, 13, 14, 15, 16, 17	LED8–15	LED driver 8–15
21	18	$\overline{\text{RESET}}$	Active low reset input
22	19	SCL	Serial clock line
23	20	SDA	Serial data line
24	21	V_{DD}	Supply voltage

BLOCK DIAGRAM

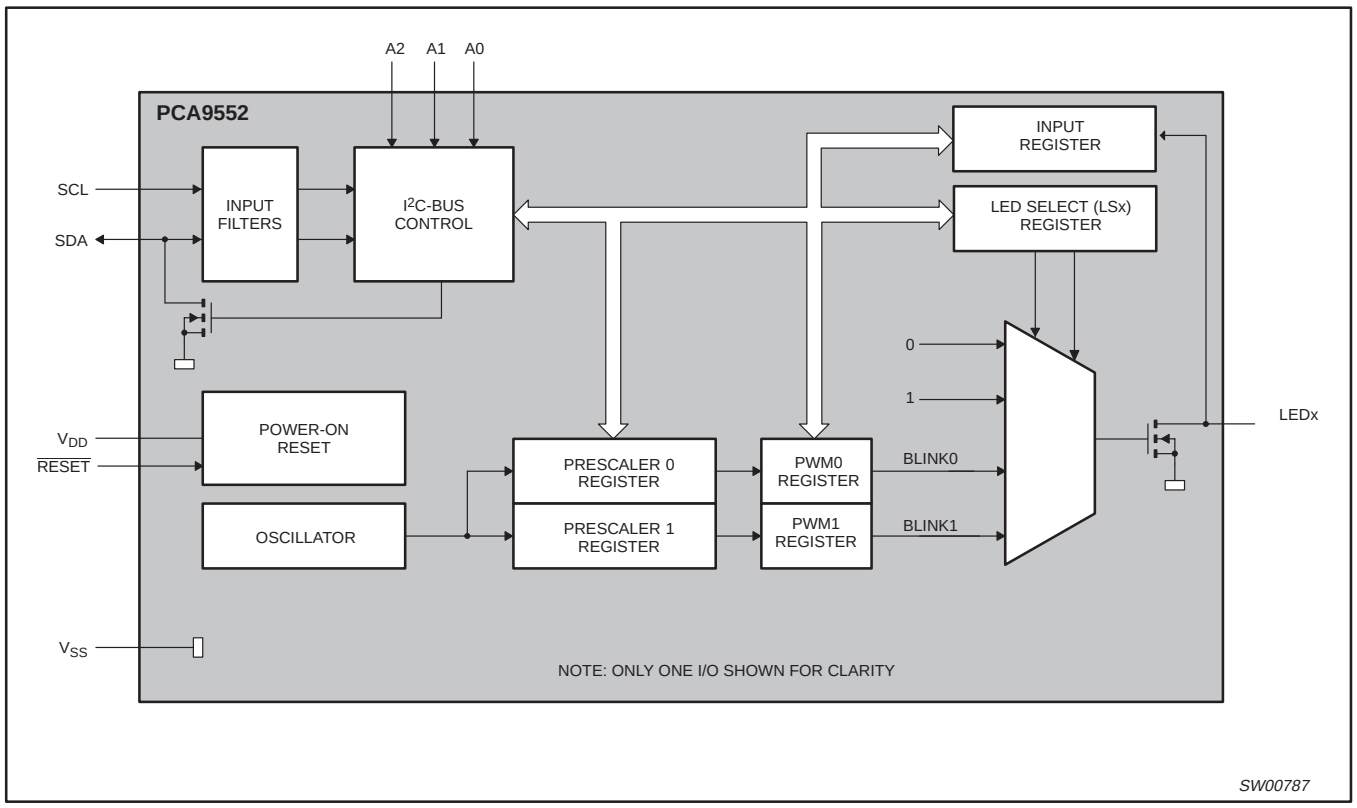


Figure 3. Block diagram

DEVICE ADDRESSING

Following a START condition the bus master must output the address of the slave it is accessing. The address of the PCA9552 is shown in Figure 4. To conserve power, no internal pullup resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

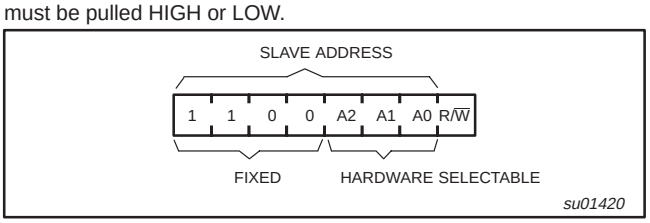


Figure 4. Slave address

The last bit of the address byte defines the operation to be performed. When set to logic 1 a read is selected while a logic 0 selects a write operation.

CONTROL REGISTER

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9552 which will be stored in the Control Register. This register can be read and written via the I²C bus.

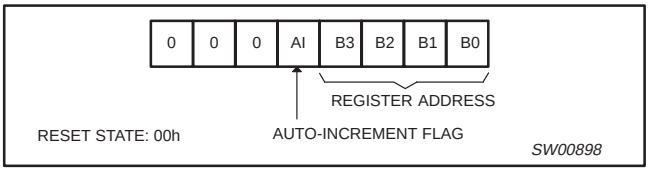


Figure 5. Control register

CONTROL REGISTER DEFINITION

B3	B2	B1	B0	REGISTER NAME	TYPE	REGISTER FUNCTION
0	0	0	0	INPUT0	READ	INPUT REGISTER 0
0	0	0	1	INPUT1	READ	INPUT REGISTER 1
0	0	1	0	PSC0	READ/ WRITE	FREQUENCY PRESCALER 0
0	0	1	1	PWM0	READ/ WRITE	PWM REGISTER 0
0	1	0	0	PSC1	READ/ WRITE	FREQUENCY PRESCALER 1
0	1	0	1	PWM1	READ/ WRITE	PWM REGISTER 1
0	1	1	0	LS0	READ/ WRITE	LED 0–3 SELECTOR
0	1	1	1	LS1	READ/ WRITE	LED 4–7 SELECTOR
1	0	0	0	LS2	READ/ WRITE	LED 8–11 SELECTOR
1	0	0	1	LS3	READ/ WRITE	LED 12–15 SELECTOR

REGISTER DESCRIPTION

The lowest 3 bits are used as a pointer to determine which register will be accessed.

If the auto-increment flag (AI) is set, the four low order bits of the Control Register are automatically incremented after a read or write. This allows the user to program the registers sequentially. The contents of these bits will rollover to '0000' after the last register is accessed.

When auto-increment flag is set (AI = 1) and a read sequence is initiated, the sequence must start by reading a register different from 0 (B3 B2 B1 B0 ≠ 0 0 0 0)

Only the 4 least significant bits are affected by the AI flag.

Unused bits must be programmed with zeroes.

INPUT0 — INPUT REGISTER 1

bit	I7	I6	I5	I4	I3	I2	I1	I0
Default	0	0	0	0	0	0	0	0

The INPUT register 1 reflects the state of the device pins (inputs 0 to 7). Writes to this register will be acknowledged but will have no effect.

INPUT1 — INPUT REGISTER 2

bit	I15	I14	I13	I12	I11	I10	I9	I8
Default	0	0	0	0	0	0	0	0

The INPUT register 1 reflects the state of the device pins (inputs 8 to 15). Writes to this register will be acknowledged but will have no effect.

PSC0 — FREQUENCY PRESCALER 0

bit	7	6	5	4	3	2	1	0
default	1	1	1	1	1	1	1	1

PSC0 is used to program the period of the PWM output.

$$\text{The period of BLINK0} = \frac{(\text{PSC0} + 1)}{38}$$

PWM0 — PWM REGISTER 0

bit	7	6	5	4	3	2	1	0
default	1	0	0	0	0	0	0	0

The PWM0 register determines the duty cycle of BLINK0. The outputs are LOW (LED off) when the count is less than the value in PWM0 and HIGH when it is greater. If PWM0 is programmed with 00h, then the PWM0 output is always LOW.

$$\text{The duty cycle of BLINK0 is:} \quad \frac{256 - \text{PWM0}}{256}$$

PSC1 — FREQUENCY PRESCALER 1

bit	7	6	5	4	3	2	1	0
default	1	1	1	1	1	1	1	1

PSC1 is used to program the period of PWM output.

$$\text{The period of BLINK1} = \frac{(\text{PSC1} + 1)}{38}$$

PWM1 — PWM REGISTER 1

bit	7	6	5	4	3	2	1	0
default	1	0	0	0	0	0	0	0

The PWM1 register determines the duty cycle of BLINK1. The outputs are LOW (LED off) when the count is less than the value in PWM1 and HIGH when it is greater. If PWM1 is programmed with 00h, then the PWM1 output is always LOW.

$$\text{The duty cycle of BLINK1 is:} \quad \frac{256 - \text{PWM1}}{256}$$

LS0 — LED 0–3 SELECTOR

	LED 3		LED 2		LED 1		LED 0	
bit	7	6	5	4	3	2	1	0
default	0	1	0	1	0	1	0	1

LS1 — LED 4–7 SELECTOR

	LED 7		LED 6		LED 5		LED 4	
bit	7	6	5	4	3	2	1	0
default	0	1	0	1	0	1	0	1

LS2 — LED 8–11 SELECTOR

	LED 11		LED 10		LED 9		LED 8	
bit	7	6	5	4	3	2	1	0
default	0	1	0	1	0	1	0	1

LS3 — LED 12–15 SELECTOR

	LED 15		LED 14		LED 13		LED 12	
bit	7	6	5	4	3	2	1	0
default	0	1	0	1	0	1	0	1

The LSx LED select registers determine the source of the LED data.

00 = Output is set low (LED on)
01 = Output is set Hi-Z (LED off – default)
10 = Output blinks at PWM0 rate
11 = Output blinks at PWM1 rate

POWER-ON RESET

When power is applied to V_{DD}, an internal Power On Reset holds the PCA9552 in a reset state until V_{DD} has reached V_{POR}. At this point, the reset condition is released and the PCA9552 registers are initialized to their default states, all the outputs in the off state.

EXTERNAL RESET

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin low for a minimum of t_W. The PCA9552 registers and I²C state machine will be held in their default state until the $\overline{\text{RESET}}$ input is once again high.

This input requires a pull-up resistor to V_{DD}.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 6).

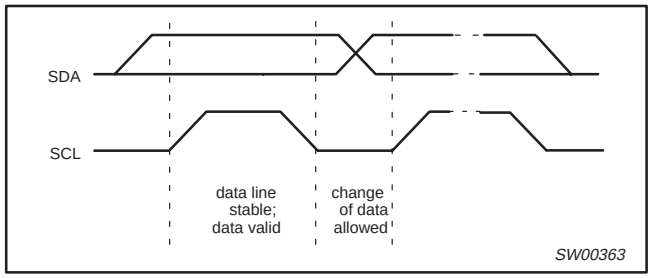


Figure 6. Bit transfer

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P) (see Figure 7).

System configuration

A device generating a message is a transmitter: a device receiving is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves (see Figure 8).

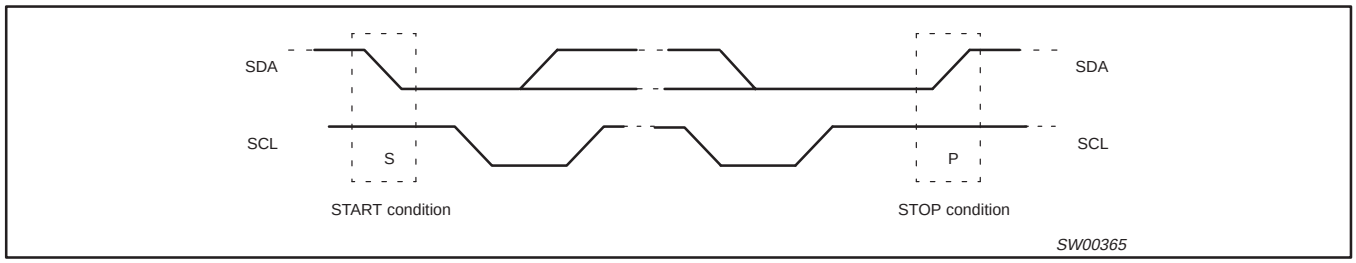


Figure 7. Definition of start and stop conditions

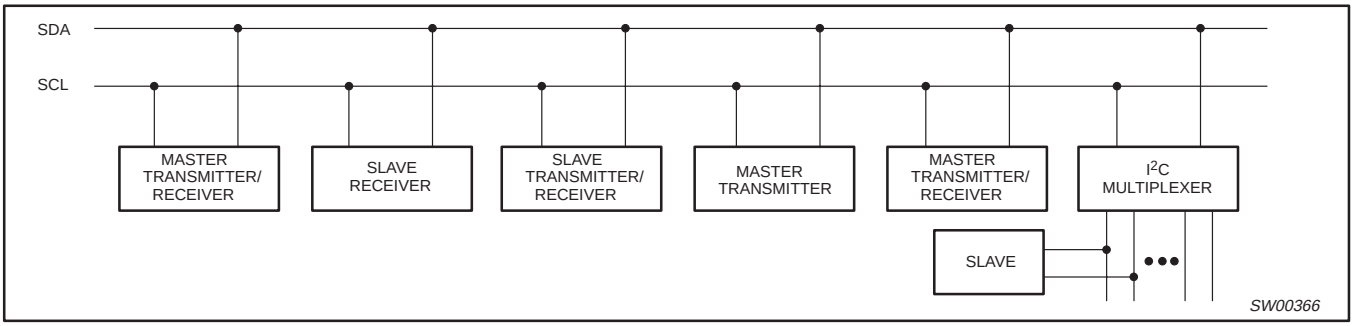


Figure 8. System configuration

Acknowledge

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

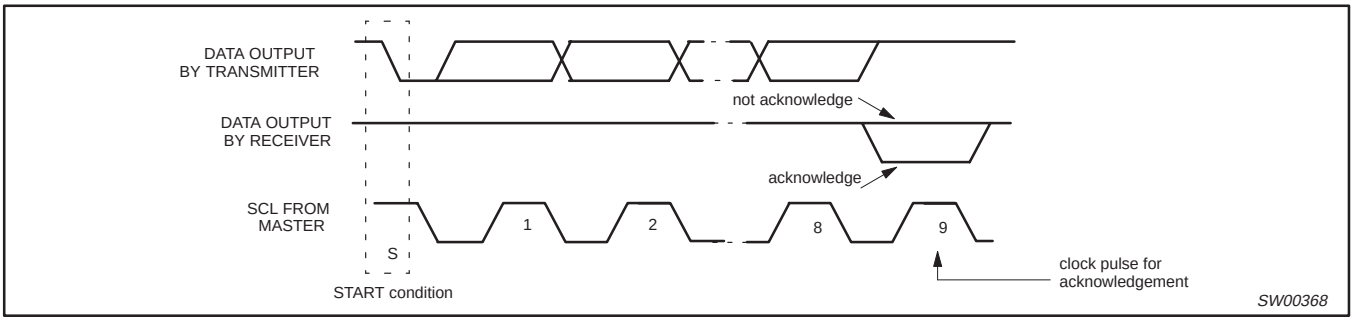


Figure 9. Acknowledgement on the I²C-bus

Bus transactions

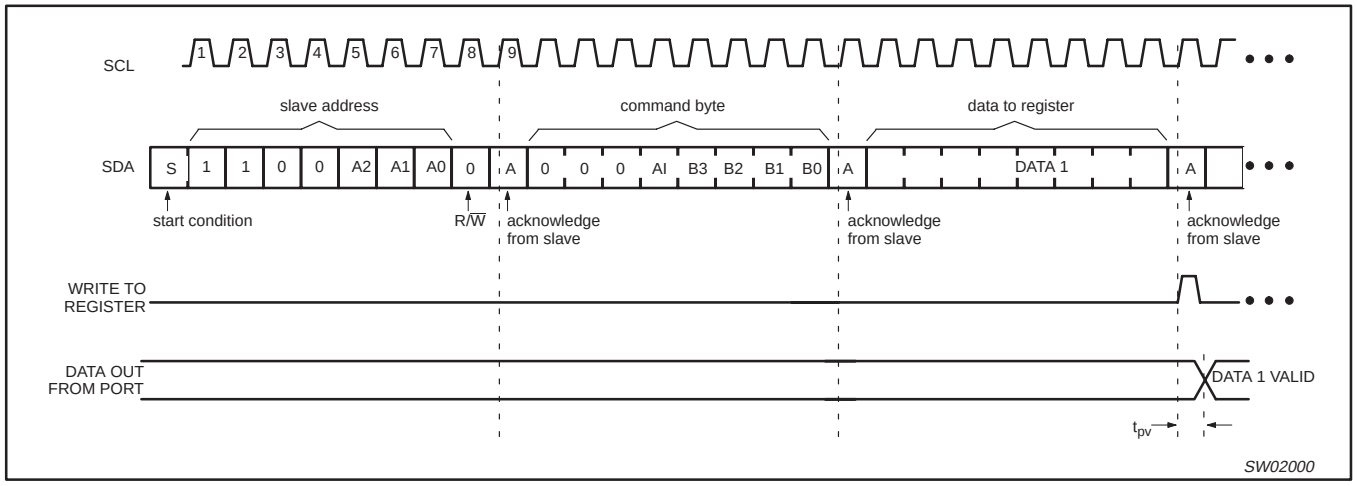


Figure 10. WRITE to register

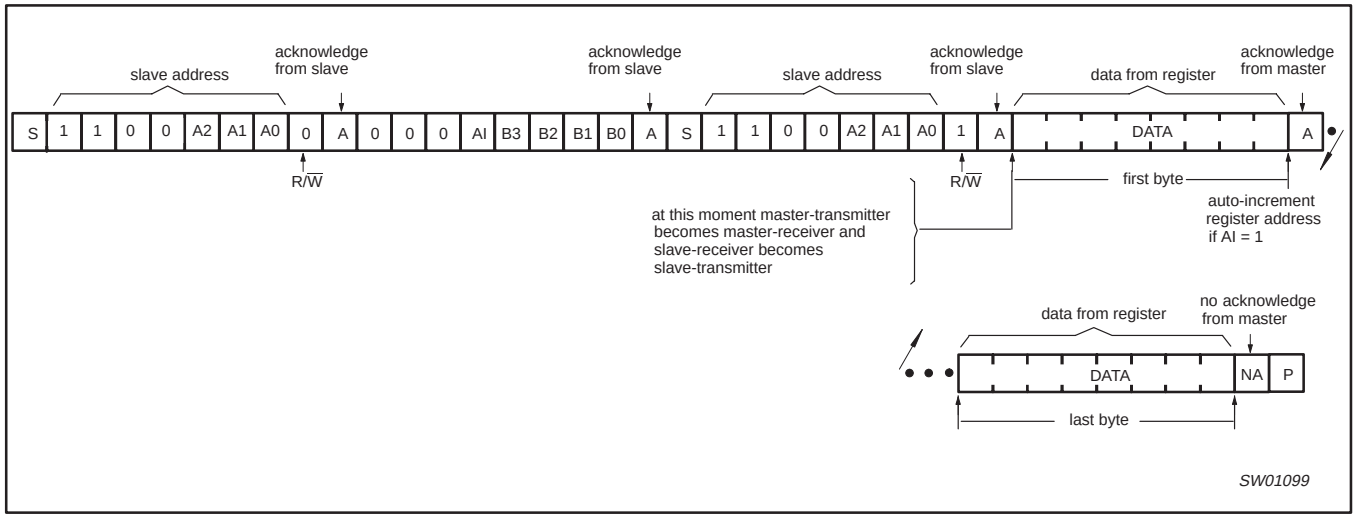
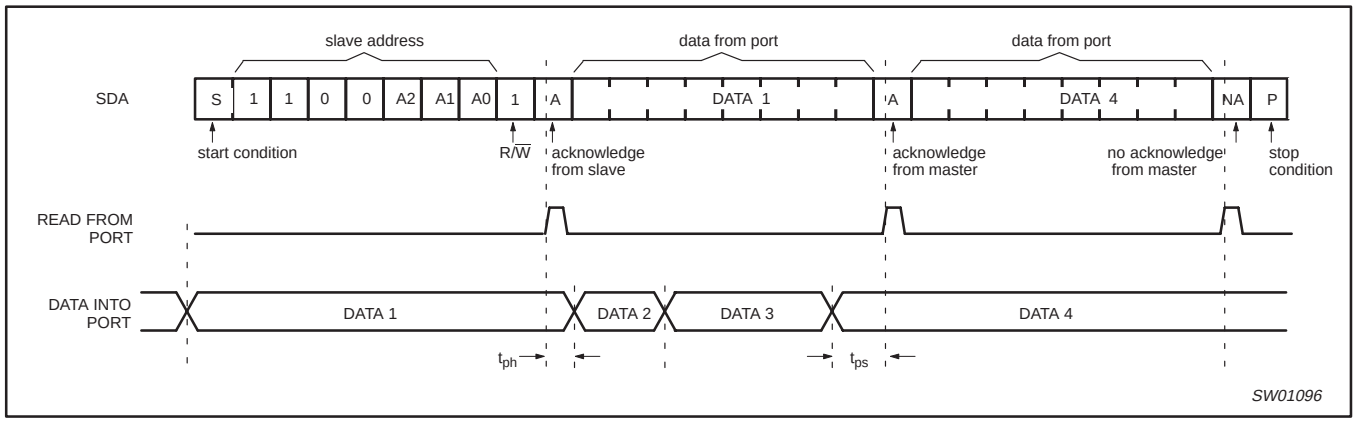


Figure 11. READ from register



NOTE:
1. This figure assumes the command byte has previously been programmed with 00h.

Figure 12. READ input port register

APPLICATION DATA

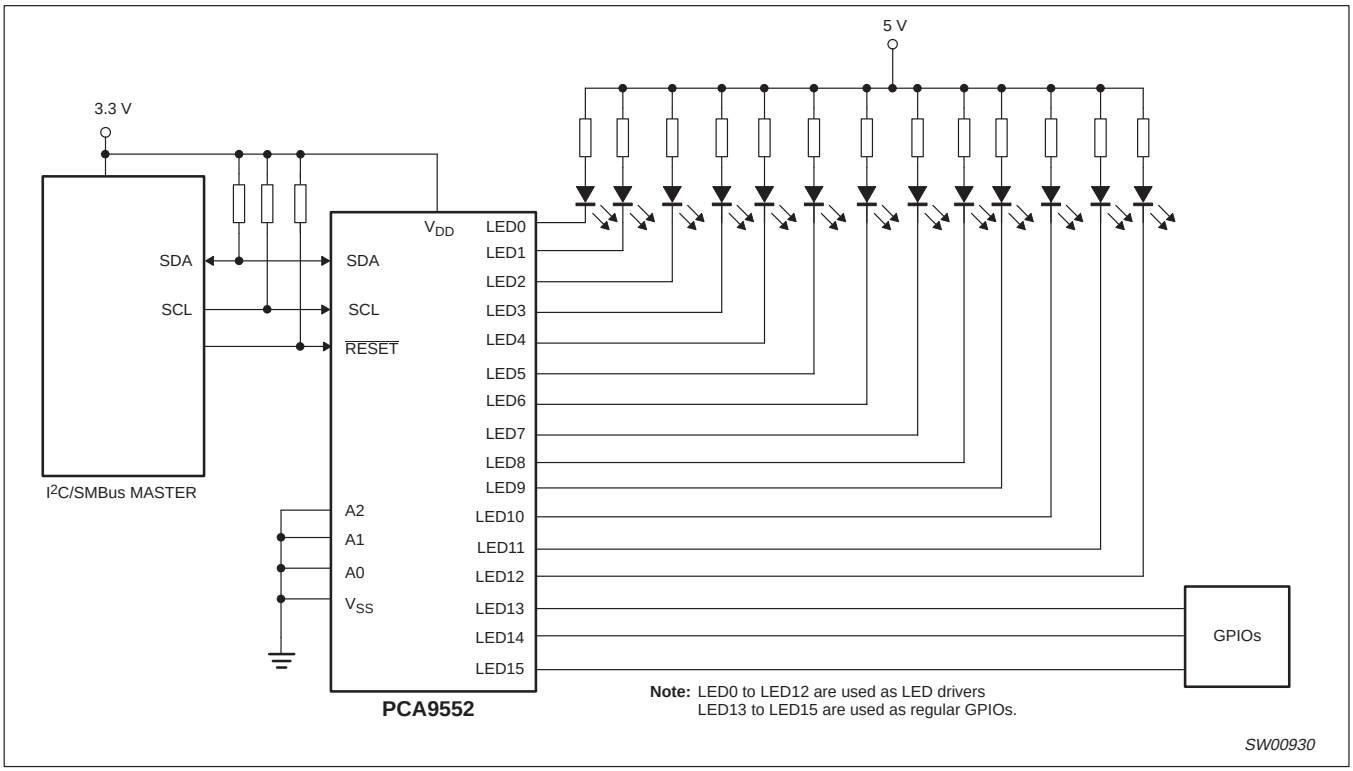


Figure 13. Typical application

Programming example

The following example will show how to set LED0 to LED3 on. It will then set LED4 and LED5 to blink at 1 Hz at a 50% duty cycle. LED6 and LED7 will be set to blink at 4 Hz and at a 25% duty cycle. LED8 to LED15 will be set to off.

Table 1.

	I²C-bus
Start	S
PCA9552 address with A0–A2 = low	C0h
PSC0 subaddress + auto-increment	12h
Set prescaler PSC0 to achieve a period of 1 second: $\text{Blink period} = 1 = \frac{PSC0 + 1}{38}$ PSC0 = 37	25h
Set PWM0 duty cycle to 50%: $\frac{256 - PWM0}{256} = 0.5$ PWM0 = 128	80h
Set prescaler PCS1 to achieve a period of 0.25 seconds: $\text{Blink period} = 0.25 = \frac{PSC1 + 1}{38}$ PSC1 = 9	09h
Set PWM1 output duty cycle to 25%: $\frac{256 - PWM1}{256} = 0.25$ PWM1 = 192	C0h
Set LED0 to LED3 on	00h
Set LED4 and 5 to PWM0, and LED6 or 7 to PWM1	FAh
Set LED8 to LED11 off	55h
Set LED12 to LED15 off	55h
Stop	P

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{DD}	Supply voltage		–0.5	6.0	V
$V_{I/O}$	DC voltage on an I/O		V_{SS} – 0.5	5.5	V
$I_{I/O}$	DC output current on an I/O		—	±25	mA
I_{SS}	Supply current		—	200	mA
P_{tot}	Total power dissipation		—	400	mW
T_{stg}	Storage temperature range		–65	+150	°C
T_{amb}	Operating ambient temperature		–40	+85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC24 under "*Handling MOS devices*".

DC CHARACTERISTICS

V_{DD} = 2.3 to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C; unless otherwise specified. TYP at 3.3 V and 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supplies						
V_{DD}	Supply voltage		2.3	—	5.5	V
I_{DD}	Supply current	Operating mode; V_{DD} = 5.5 V; no load; $V_I = V_{DD}$ or V_{SS}; f_{SCL} = 100 kHz	—	350	550	µA
I_{stb}	Standby current	Standby mode; V_{DD} = 5.5 V; no load; $V_I = V_{DD}$ or V_{SS}; f_{SCL} = 0 kHz	—	2.1	5.0	µA
V_{POR}	Power-on reset voltage	V_{DD} = 3.3 V; no load; $V_I = V_{DD}$ or V_{SS}	—	1.7	2.2	V
Input SCL; input/output SDA						
V_{IL}	LOW level input voltage		–0.5	—	0.3 V_{DD}	V
V_{IH}	HIGH level input voltage		0.7 V_{DD}	—	5.5	V
I_{OL}	LOW level output current	V_{OL} = 0.4V	3	6.5	—	mA
I_L	Leakage current	$V_I = V_{DD} = V_{SS}$	–1	—	+1	µA
C_I	Input capacitance	$V_I = V_{SS}$	—	4.4	5	pF
I/Os						
V_{IL}	LOW level input voltage		–0.5	—	0.8	V
V_{IH}	HIGH level input voltage		2.0	—	5.5	V
I_{OL}	LOW level output current	V_{OL} = 0.4 V; V_{DD} = 2.3 V; Note 1	9	14	—	mA
		V_{OL} = 0.4 V; V_{DD} = 3.0 V; Note 1	12	18	—	mA
		V_{OL} = 0.4 V; V_{DD} = 5.0 V; Note 1	15	22	—	mA
		V_{OL} = 0.7 V; V_{DD} = 2.3 V; Note 1	15	22	—	mA
		V_{OL} = 0.7 V; V_{DD} = 3.0 V; Note 1	20	28	—	mA
		V_{OL} = 0.7 V; V_{DD} = 5.0 V; Note 1	25	38	—	mA
I_L	Input leakage current	V_{DD} = 3.6 V; V_I = 0 or V_{DD}	–1	—	1	µA
C_{IO}	Input/output capacitance		—	2.6	5	pF
Select Inputs A0, A1, A2 / $\overline{\text{RESET}}$						
V_{IL}	LOW level input voltage		–0.5	—	0.8	V
V_{IH}	HIGH level input voltage		2.0	—	5.5	V
I_{LI}	Input leakage current		–1	—	1	µA
C_I	Input capacitance	$V_I = V_{SS}$	—	2.3	5	pF

NOTES:

1. The total current sunk for all I/Os must be limited to 200 mA and 25 mA per I/O.

AC SPECIFICATIONS

SYMBOL	PARAMETER	STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNITS
		MIN	MAX	MIN	MAX	
f_{SCL}	Operating frequency	0	100	0	400	kHz
t_{BUF}	Bus free time between STOP and START conditions	4.7	—	1.3	—	µs
$t_{HD;STA}$	Hold time after (repeated) START condition	4.0	—	0.6	—	µs
$t_{SU;STA}$	Repeated START condition setup time	4.7	—	0.6	—	µs
$t_{SU;STO}$	Setup time for STOP condition	4.0	—	0.6	—	µs
$t_{HD;DAT}$	Data in hold time	0	—	0	—	ns
$t_{VD;ACK}$	Valid time for ACK condition[2]	—	600	—	600	ns
$t_{VD;DAT}$ (L)	Data out valid time[3]	—	600	—	600	ns
$t_{VD;DAT}$ (H)	Data out valid time[3]	—	1500	—	600	ns
$t_{SU;DAT}$	Data setup time	250	—	100	—	ns
t_{LOW}	Clock LOW period	4.7	—	1.3	—	µs
t_{HIGH}	Clock HIGH period	4.0	—	0.6	—	µs
t_F	Clock/Data fall time	—	300	20 + 0.1 C_b[1]	300	ns
t_R	Clock/Data rise time	—	1000	20 + 0.1 C_b[1]	300	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filters	—	50	—	50	ns
Port Timing						
t_{PV}	Output data valid	—	200	—	200	ns
t_{PS}	Input data setup time	100	—	100	—	ns
t_{PH}	Input data hold time	1	—	1	—	µs
Reset						
t_W	Reset pulse width	10	—	10	—	ns
t_{REC}	Reset recovery time	0	—	0	—	ns
t_{RESET}[4,5]	Time to reset	400	—	400	—	ns

NOTES:
1. C_b = total capacitance of one bus line in pF.
2. $t_{VD;ACK}$ = time for Acknowledgement signal from SCL low to SDA (out) low.
3. $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL low.
4. Resetting the device while actively communicating on the bus may cause glitches or errant STOP conditions.
5. Upon reset, the full delay will be the sum of t_{RESET} and the RC time constant of the SDA bus.

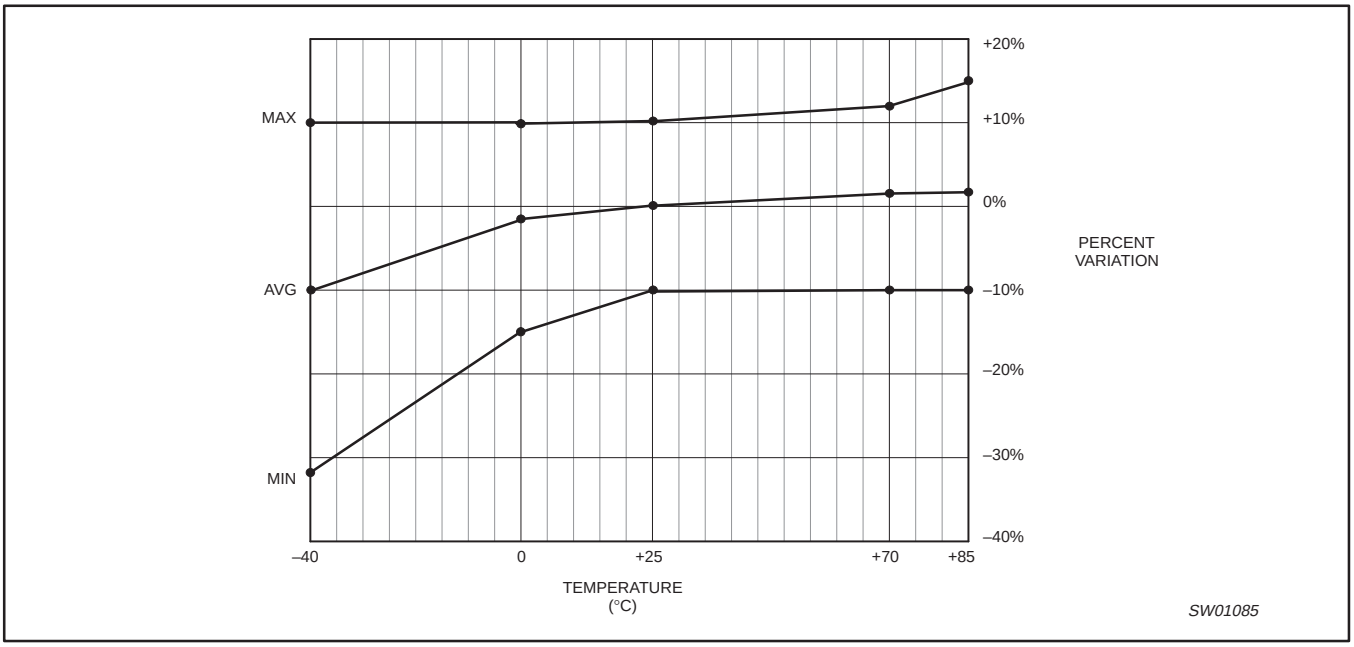


Figure 14. Typical frequency variation over process at V_{DD} = 2.3 V to 3.0 V

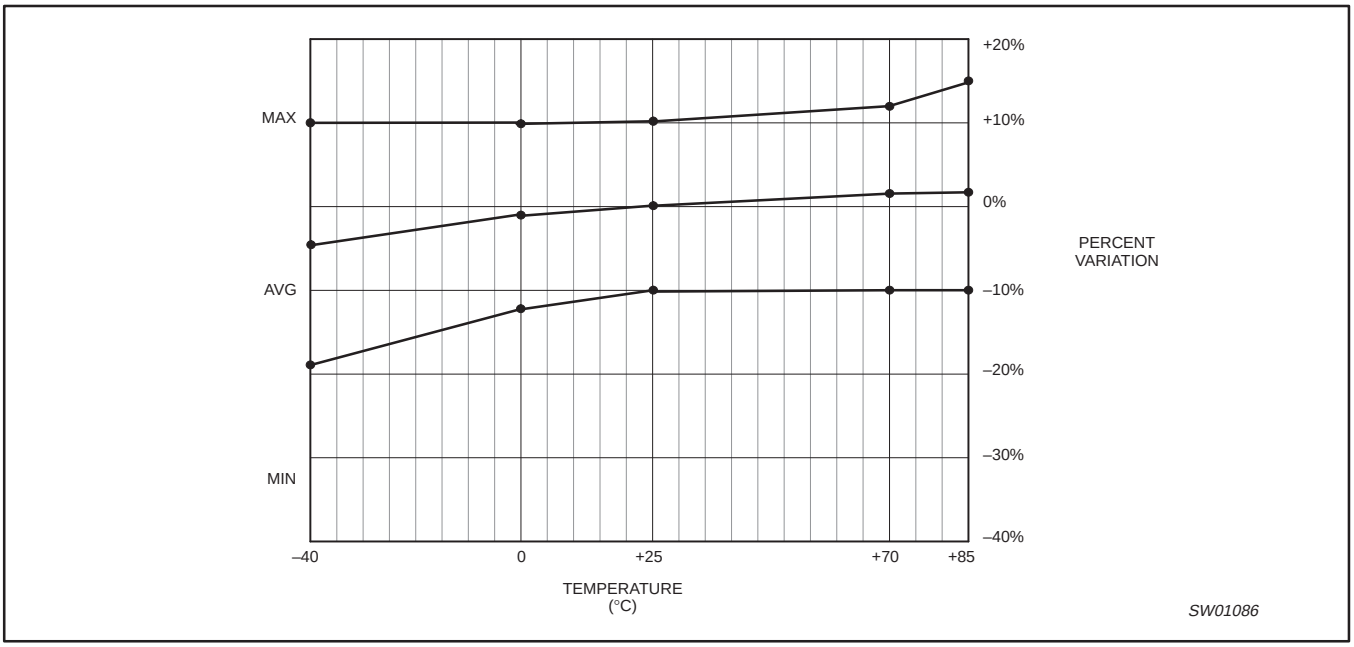


Figure 15. Typical frequency variation over process at V_{DD} = 3.0 V to 5.5 V

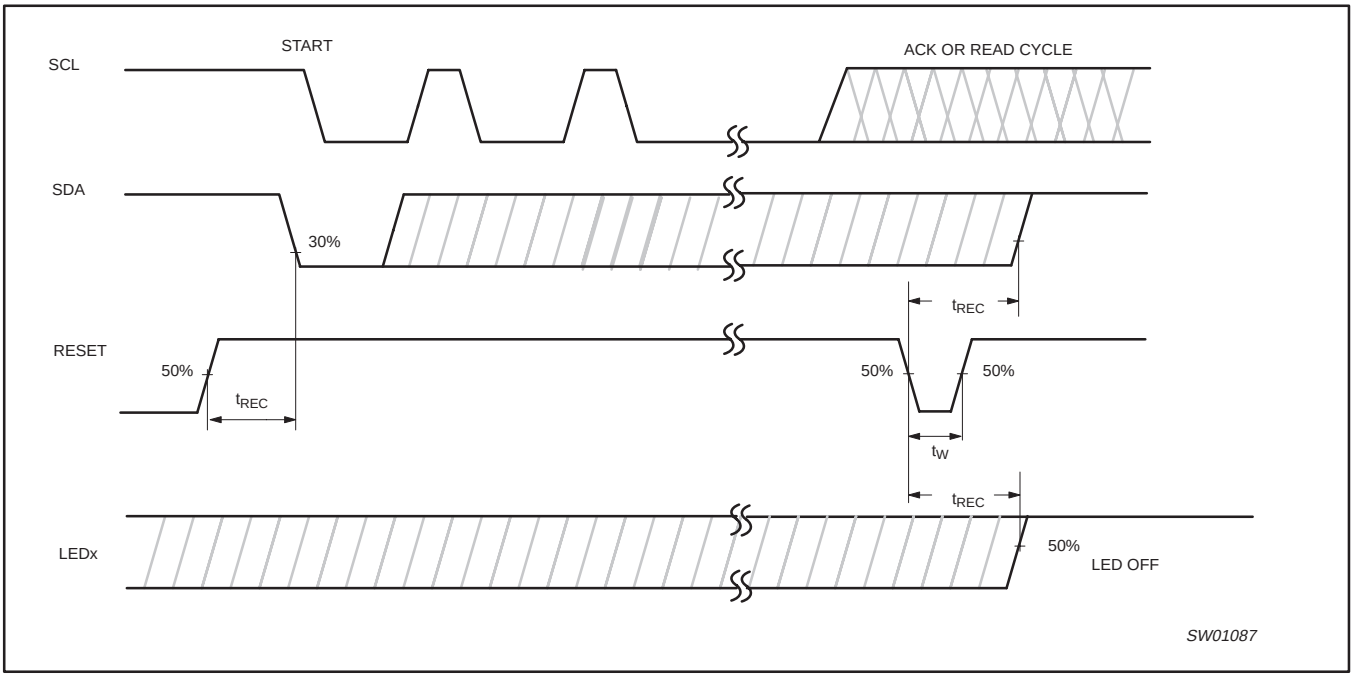


Figure 16. Definition of $\overline{\text{RESET}}$ timing

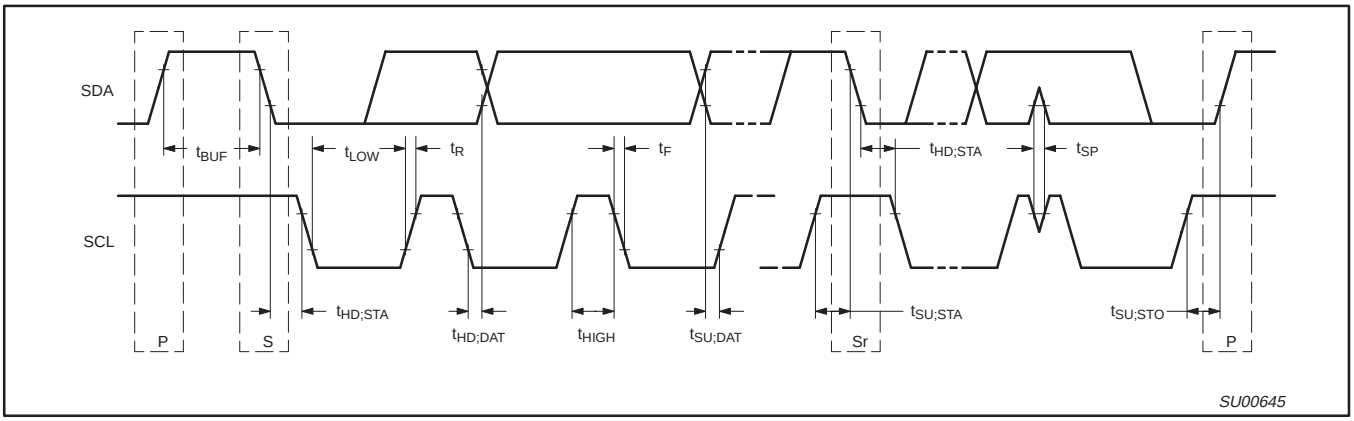
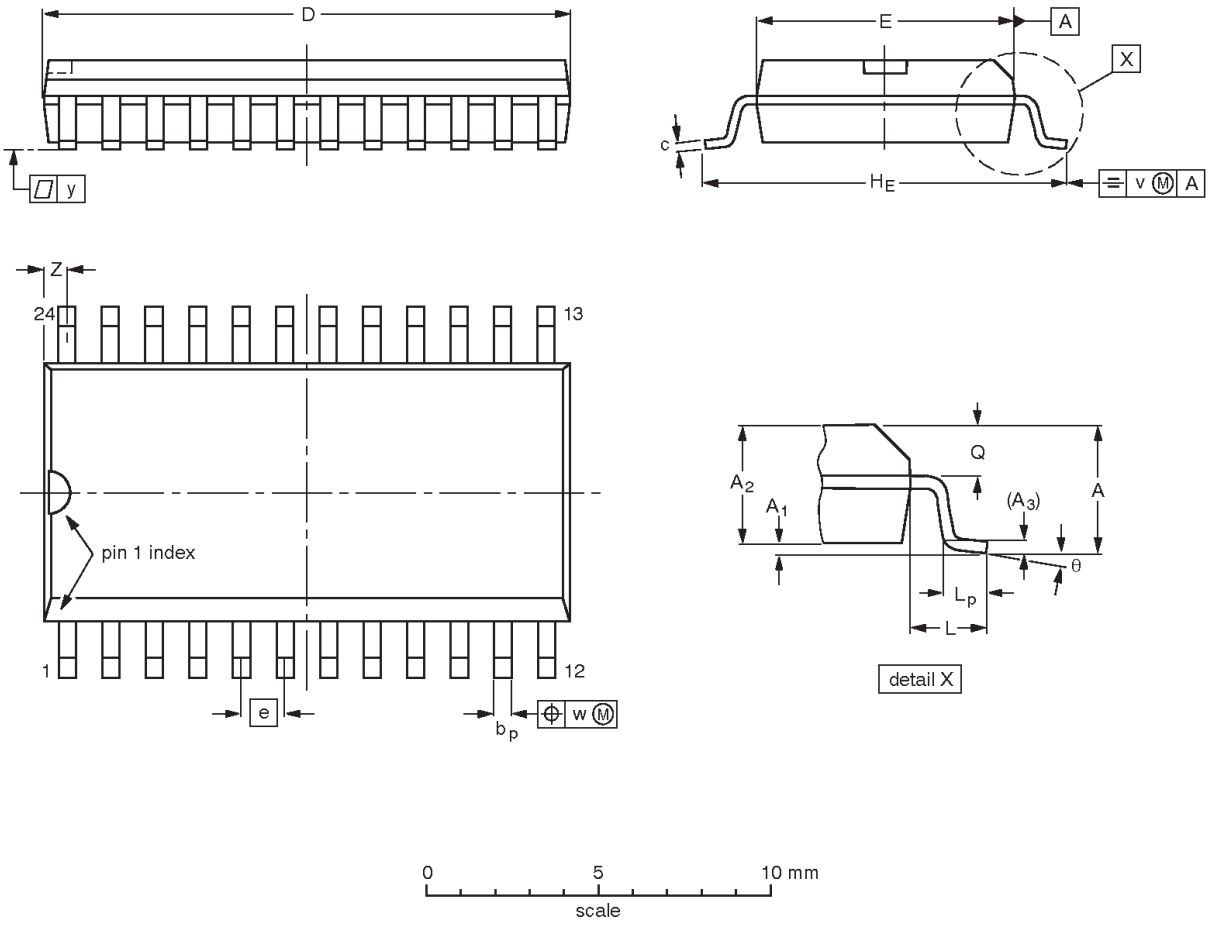


Figure 17. Definition of timing

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

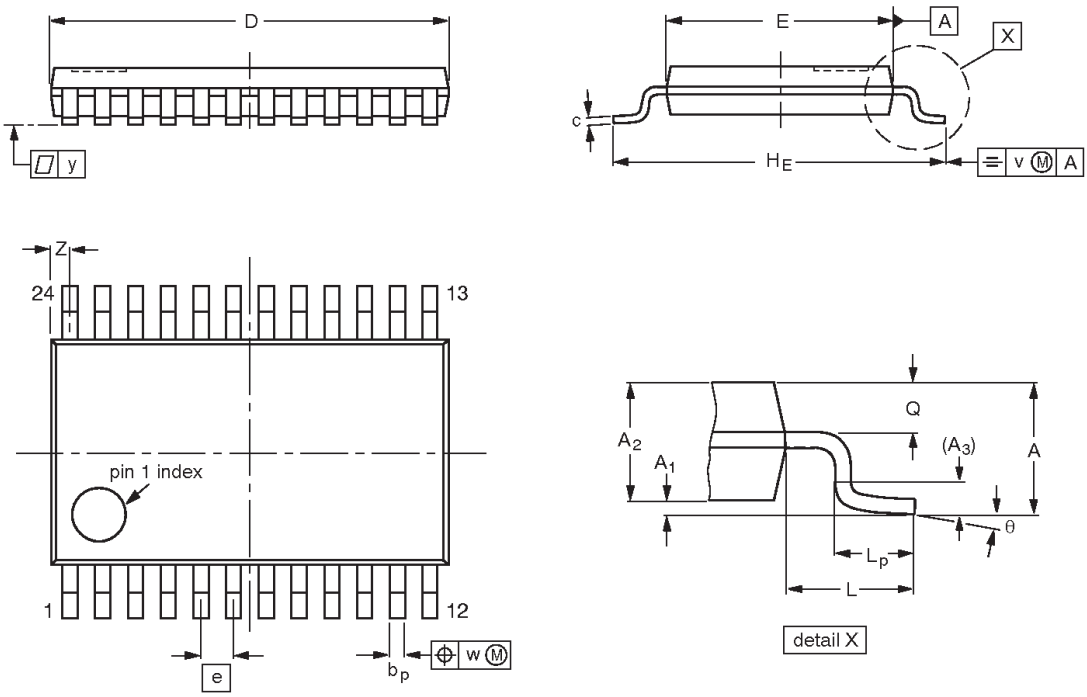
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

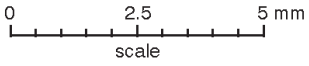
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013				~~97-05-22~~ 99-12-27

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**





DIMENSIONS (mm are the original dimensions)

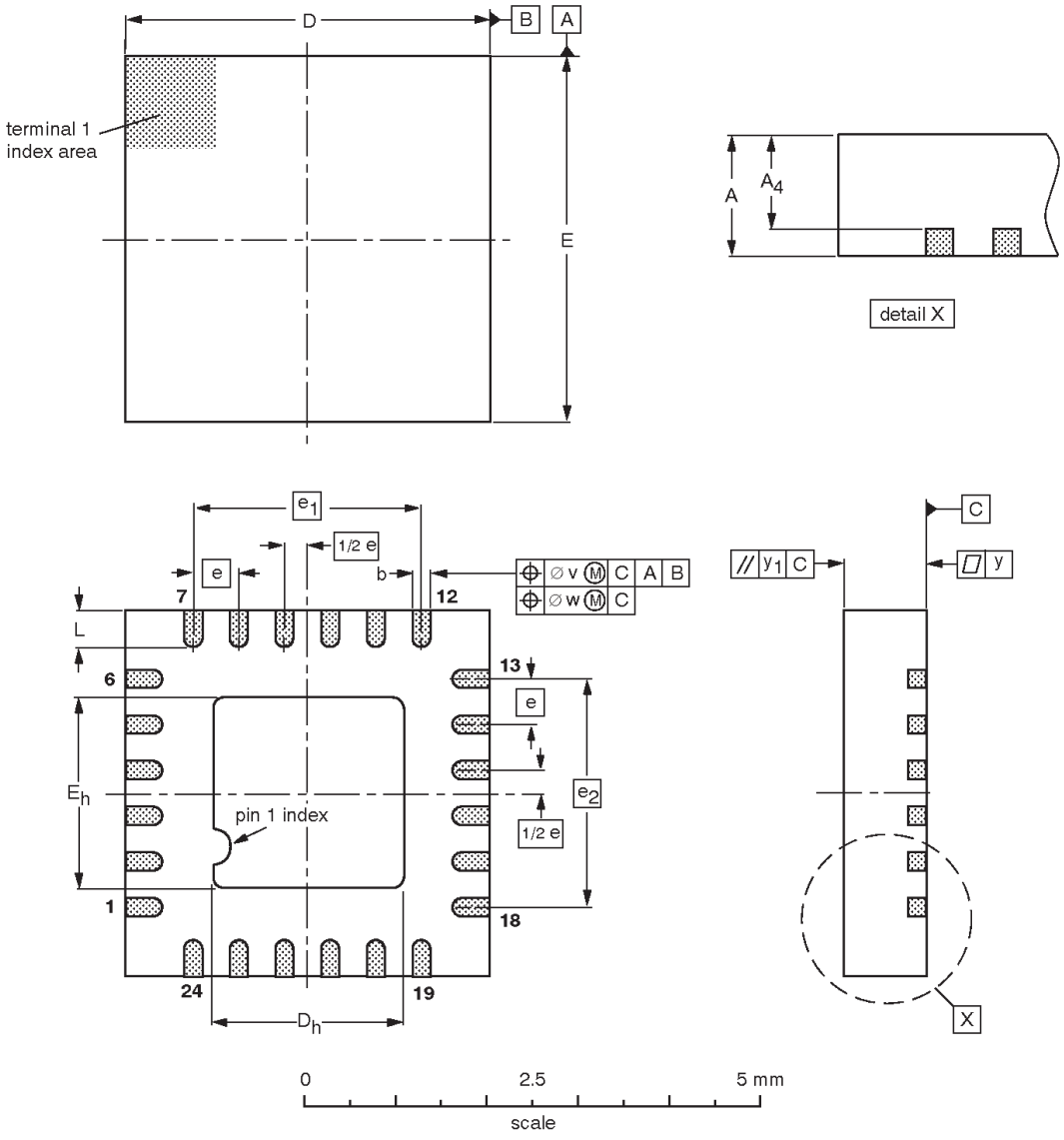
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153				~~95-02-04~~ 99-12-27

HVQFN24: plastic, heatsink very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm **SOT616-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_4 max.	b	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1.00	0.80	0.35 0.18	4.05 3.95	2.25 1.95	4.05 3.95	2.25 1.95	0.5	2.5	2.5	0.50 0.30	0.2	0.1	0.05	0.1

Note

1. Plastic or metal protrusions of 0.076 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT616-1		MO-220				~~01-06-07~~ 01-08-08

REVISION HISTORY

Rev	Date	Description
_1	2002 Sep 27	Product data (9397 750 10329); initial version Engineering Change Notice: 853–2374 28878 (2002 Sep 09)

16-bit I²C LED driver with programmable blink rates PCA9552

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

Data sheet status

Data sheet status[1]	Product status[2]	Definitions
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Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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