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# Atmel AVR1020: Migration from ATxmega256A3/192A3/128A3/64A3 to ATxmega256A3U/192A3U/128A3U/64A3U



## Features

- Enhancement and added functions
- Memories
- System clock and clock options
- Reset sources
- I/O ports
- DAC – digital to analog converter
- AC – analog comparator

## 1 Introduction

This application note is a guide to assist users of Atmel ATxmega256A3/192A3/128A3/64A3 in converting designs to Atmel ATxmega256A3U/192A3U/128A3U/64A3U. For complete device details, always refer to the most recent version of the ATxmega256A3U/192A3U/128A3U/64A3U datasheet and the Atmel® AVR® XMEGA® AU manual. Errata differences between ATxmega256A3/192A3/128A3/64A3 and ATxmega256A3U/192A3U/128A3U/64A3U are not listed in this document, only in the device datasheet.

In addition to the differences described in this document, other typical characteristics could be different. Please check the latest datasheet for details.

ATxmega256A3U/192A3U/128A3U/64A3U also includes new configuration options and functions. As far as possible these are implemented as a superset of existing ATxmega256A3/192A3/128A3/64A3 functions, so existing code for these devices will work on the new devices without changing existing configuration or enabling new functions. The new options and functions are listed in the application note for customers who in addition to a pure migration also wish to see an overview to consider use of the new functions.

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**8-bit Atmel  
Microcontrollers**

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**Application Note**

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## 2 Enhancements and added functions

In this section, we summarize the enhancement or added features in Atmel ATxmega256A3U/192A3U/128A3U/64A3U compared to Atmel ATxmega256A3/192A3/128A3/64A3. For pure migration, you can skip the section and start from the next section.

### 2.1 USB

- One USB 2.0 full speed (12Mbps) and low speed (1.5Mbps) device compliant interface is added

### 2.2 Clock system

- A divide-by-two option for the PLL output that enables output frequency down to 10MHz
- PLL lock failure detection with optionally Non-Maskable Interrupt (NMI), for improved safety and robustness
- Non-prescaled Real Time Counter clock source options: External clock from TOSC1, 32.768kHz from TOSC, and the 32.768kHz from the 32.768kHz Internal Oscillator
- Higher drive option for external crystal oscillator to support crystals with higher load
- The 32MHz Internal Oscillator can be tuned to run at any frequency between 30MHz and 55MHz

### 2.3 Two wire interface

- The SDA Hold time can be increased and configured in order to be SMBUS compliant

### 2.4 I/O ports

- Alternate pin locations for Timer/Counter 0 Compare Channels, USART0 and SPI
- Alternate pin locations for the Peripheral Clock and Event output functions
- The Real Time Counter clock can be output to a port pin
- Any Event Channel can be output to a port pin

### 2.5 Analog to digital converter

- Automatic input channel scan
- VCC/2 voltage reference option
- 1/2x (divide by two) gain stage setting
- Internal ground can be used as negative input in differential mode (with gain)

### 2.6 Analog comparator

- Analog Comparator 1 can be output on a port pin
- A constant current source

## 2.7 CRC16/CRC32 generator

- A CRC16/CRC32 Generator Module that supports CRC16 (RC-CCITT) and CRC-32 (IEEE 802.3)

## 2.8 16-bit timer/counter0

- Split mode that enable two 8-bit Timer/Counters with 4 PWM channels each

## 2.9 High resolution extension

- Hi-Res+ option to allow PWM resolution to be increased with 8x (3-bit)

## 2.10 Power management

- Possibility to enable sequential start of the components used for analog modules ADC and Analog Comparator in order to reduce start-up current

## 3 Memories

### 3.1 NVM controller

For Atmel ATxmega256A3U/192A3U/128A3U/64A3U devices, the chip erase time is about 40ms. The chip erase time of Atmel ATxmega256A3U/192A3U/128A3U/64A3U devices is longer.

The typical chip erase time of ATxmega256A3U/192A3U/128A3U/64A3U devices is listed in the table below.

**Table 3-1.** ATxmega256A3U/192A3U/128A3U/64A3U chip erase time.

Product	Flash and boot code size	Chip erase time
ATxmega64A3U	64KB + 4KB	55ms
ATxmega128A3U	128KB + 8KB	75ms
ATxmega192A3U	192KB + 8KB	90ms
ATxmega256A3U	256KB + 8KB	105ms

To ensure that the flash chip erase be finished correctly, no flash access should be done during the chip erase time.

In the user code, it is always needed to check the FBUSY bit in Non-Volatile Memory Status Register to see when the chip erase is finished.

### 3.2 Fuses and lock bits

BOD levels are different in ATxmega256A3U/192A3U/128A3U/64A3U. Please see section 5.1 Brown-Out Detection for the differences.





## 4 System clock and clock options

### 4.1 DFLL 2MHz and DFLL 32MHz

COMP0, the lowest byte of Oscillator Compare Register, does not exist from both DFLLs for 2MHz and 32MHz internal oscillator in Atmel ATxmega256A3U/192A3U/128A3U/64A3U. For more details, please refer to device datasheet.

## 5 Reset source

### 5.1 Brown-out detection

The programmable BODLEVEL settings are different in Atmel ATxmega256A3U/192A3U/128A3U/64A3U. See [Table 5-1](#) below for details. Please refer to the device datasheet regarding tolerance for the Brown-out levels.

**Table 5-1.** Brown-out levels.

BODLEVEL	VBOT - XMEGA AU	VBOT - XMEGA A
111	1.6V	1.6V
110	1.8V	1.9V
101	2.0V	2.1V
100	2.2V	2.4V
011	2.4V	2.6V
010	2.6V	2.9V
001	2.8V	3.2V
000	3.0V	3.4V

## 6 I/O ports

The I/O port pins are LVTTTL and LVCMOS compatible for Atmel ATxmega256A3U/192A3U/128A3U/64A3U devices. The minimum “Input High Voltage” is never higher than 2.0V for  $VCC > 2.7V$ .

In Atmel ATxmega256A3/192A3/128A3/64A3, the minimum “Input High Voltage” is 0.7VCC, and could be higher than 2.0V for  $VCC > 2.86V$ .

## 7 DAC – digital to analog converter

The Atmel ATxmega256A3U/192A3U/128A3U/64A3U DAC has two continuous output channels, and not a sample and hold circuit as Atmel ATxmega256A3/192A3/128A3/64A3 devices. This give continuous time output and higher sample rate for each channel. There is separate calibration (offset/gain) for each DAC channel in ATxmega256A3U/192A3U/128A3U/64A3U.

When DACA0OFFCAL (in Production Signature Row) is written to CH0OFFSETCAL in DACA, CH1OFFSETCAL is also written with this value. The details of this operation are shown below.

The first step,

- read DACA0OFFCAL from production signature row
- write DACA0OFFCAL to DACA.CH0OFFSETCAL

This will result in:

- DACA.CH0OFFSETCAL = DACA0OFFCAL
- DACA.CH1OFFSETCAL = DACA0OFFCAL

The second step,

- read DACA1OFFCAL from production signature row
- write DACA1OFFCAL to DACA.CH1OFFSETCAL

This will result in:

- DACA.CH1OFFSETCAL = DACA1OFFCAL

After that, any further writing to DACA.CH0OFFSELCAL does not change DACA.CH1OFFSELCAL until the next reset. The same is implemented for both OFFSET and GAIN calibration registers in DACA and DACB. This ensure that customers using the ATxmega256A3/192A3/128A3/64A3 DAC can continue and use the same calibration sequence and still calibrate both channels.

TIMCTRL register does not exist in ATxmega256A3U/192A3U/128A3U/64A3U, so there are no timing constraints on DAC operation.

## 8 AC – analog comparator

In Atmel ATxmega256A3U/192A3U/128A3U/64A3U, there is a two-cycle delay from writing a new MUX setting until it takes effect.



## 9 Registers

### 9.1 Removed registers and bits

The below table lists register bits, which exist in Atmel ATxmega256A3/192A3/128A3/64A3 but not in Atmel ATxmega256A3U/192A3U/128A3U/64A3U.

**Table 9-1.** Register bits and functionality that does not exist in ATxmega256A3U/192A3U/128A3U/64A3U.

Register name	Register bit	Function
TIMCTRL	CONINTVAL[2:0]	DAC Conversion Interval
	REFRESH[3:0]	DAC Channel Refresh Timing Control
COMP0	COMP[7:0]	Oscillator Compare Register 0

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